THERMAL CHARACTERISATION AND RELIABILITY ANALYSIS OF POWER ELECTRONIC DEVICES IN WIND AND SOLAR ENERGY SYSTEMS

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THERMAL CHARACTERISATION AND RELIABILITY ANALYSIS OF POWER ELECTRONIC DEVICES IN WIND AND SOLAR ENERGY SYSTEMS

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Abstract

Power electronic converters (PECs) are used for conditioning the flow of energy between renewable energy applications and grid or stand-alone connected loads. Insulated gate bipolar transistors (IGBTs) are critical components used as switching devices in PECs. IGBTs are multi-layered devices made of different coefficient of thermal expansion (CTE) based materials.

In wind and solar energy applications, IGBT's reliability is highly influenced by the operating conditions such as variable wind speed and solar irradiance. Power losses occur in switching transient of high current/voltage which causes temperature fluctuations among the layers of the IGBTs. This is the main stress mechanism which accelerates deterioration and eventual failures among IGBT layers due to the dissimilar CTEs. Therefore, proper thermal monitoring is essential for accurate estimation of PECs reliability and end lifetime.

Several thermal models have been proposed in literature, which are not capable of representing accurate temperature profiles among multichip IGBTs. These models are mostly derived from offline modelling approaches which cannot take operating conditions and control mechanisms of PECs into account and unable to represent actual heat path among each chip.

This research offers an accurate and powerful electro thermal and reliability monitoring tool for such devices. Three-dimensional finite element (FE) IGBT models are implemented using COMSOL, by considering complex heat interactions among each layer. Based on the obtained thermal characteristics, electro thermal and thermo mechanical models were developed in SIMULINK to determine the thermal behaviour of each layer and provide total lifetime consumption analysis. The developed models were verified by real-time (RT) experiments using dSPACE environment.

New materials, such as silicon carbide (SiC) devices, were found to exhibit approximately 20°C less thermal profile compared to conventional silicon IGBTs. For PECs used within wind energy systems, PECs driving algorithms were derived within the proposed models and by adjusting switching frequency PECs cycling temperatures were reduced by 12°C which led to a significant reduction in thermal stress; approximately 27 MPa. Total life consumption for the proposed method was calculated as 3.26×10^{-5} which is approximately 1×10^{-5} less compared to the other both methods. Effects of maximum power tracking algorithms, used in photovoltaic solar systems, on thermal stress were also explored. The converter's thermal cycling was found approximately 3 °C higher with the IC algorithm. The steady state temperature was 52.7°C for the IC while it was 42.6 °C for P&O. In conclusion, IC algorithm offers more accurate tracking accuracy; however, this is on the expense of harsher thermal stress which has led to approximately 1.4 times of life consumption compared to P&O under specific operating conditions.

Declaration

No portion of the work referred in this thesis has been submitted in support of an application for another degree or qualification at this, or any other university, or institute of learning.

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Abbreviation

2L-BTBC	Two Level Back to Back Converter
3L-NPCC	Three Level Neutral Point Clamped Converter
AC	Alternating Current
ALEC	Aluminium Electrolytic Capacitors
CB-SVPWM	Carrier Based Space Vector Pulse Width Modulation
CCM	Continuous Conduction Mode
CFD	Computational Fluid Dynamics
CTE	Coefficient of Thermal Expansion
DC	Direct Current
DCTM	Dynamic Compact Thermal Models
DFIG	Doubly Fed Induction Generator
DFR	Design for Reliability
DSP	Digital Signal Processing
ECU	Electronic Control Unit
ESR	Effective Series Resistance
FE	Finite Element
FEM	Finite Element Model
FPGA	Field Programmable Gate Array
FS	Full Scale
FSTP	Field Stop
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GTO	Gate Turn Off Thyristor
HCI	Hot Carrier Injection
IC	Incremental Conductance
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
LCM	Life Cycle Management
MTBF	Mean Time Between Failures
MLCC	Multi-Layer Ceramic Capacitors
MPPT	Maximum Power Point Tracking

MPPFC	Metallized Polypropylene Film Capacitors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability
NPT	Non-Punch Through
PECs	Power Electronic Converters
PMG	Permanent Magnet Generator
PS	Partial Scale
PT	Punch-Through
P&O	Perturb and Observe
PWM	Pulse Width Modulation
PV	Photovoltaic
RES	Renewable Energy Sources
RoHS	Restriction of Hazardous Substances
RTI	Real Time Interface
SiC	Silicon Carbide
SCR	Silicon-Controlled Rectifiers
SA	Shorted Anode
SJFS	Super Junction Field Stop
SPT	Soft-Punch Through
SPWM	Sinusoidal Pulse Width Modulation
SSM	Small Signal Modelling
SVM	State Vector Modulation
TDDB	Time Dependent Dielectric Breakdown
THIPWM	Third Harmonic Pulse Width Modulation
VSC	Voltage Source Converter
WRIG	Wound Rotor Induction Generator

List of Publications based on this Work

C. Batunlu and A. Albarbar, “Real-time system for monitoring the electro-thermal behaviour of power electronic devices used in boost converters,” Microelectron. Reliab., vol. 62, pp. 82–90, July 2016.

C. Batunlu and A. Albarbar, “Towards More Reliable Renewable Power Systems - Thermal Performance Evaluation of DC/DC Boost Converters Switching Devices,” Int. J. Power Electron. Drive Syst. IJPEDS, vol. 6, no. 4, pp. 876–887, Dec. 2015.

C. Batunlu and A. Albarbar, “A Technique for Mitigating Thermal Stress and Extending Life Cycle of Power Electronic Converters Used for Wind Turbines,” Electronics, vol. 4, no. 4, pp. 947–968, Nov. 2015.

C. Batunlu and M. Musallam, “3D thermal model of power electronic conversion systems for wind energy applications,” in 2014 IEEE Global Humanitarian Technology Conference (GHTC), 2014, pp. 369–376.

C. Batunlu and M. Musallam, “Electro-Thermal Analysis of Conversion Systems for Wind Energy Applications,” in 2013 Building a Smart Power Future (iPower3).

C. Batunlu and A. Albarbar, “An Investigation into the Lifetime of Power Electronics in Solar Photovoltaic Systems under Different Maximum Power Point Tracking Algorithms”, IEEE Trans. of Power Electronics, Under review

C. Batunlu and A. Albarbar, “Reliability Estimations of a DC/AC Inverter Power Module for Wind Energy Applications”, Under preparation

Chapter 1

Introduction to the Proposed Research

1.1 Motivation

Renewable energy sources (RESs) have recently been playing a significant role in electricity generation. Power electronic converters (PECs) interface renewable energy generators (such as solar panels and wind turbines) to utility grid for conditioning of the energy flow (i.e. voltage and frequency regulation) and safety [1]. However, high and random variations in wind speeds and solar irradiations have huge impact on total amount of generated energy. Hence, unpredictable temperature profile occurs within the associated power electronic converters (PECs). This causes difficulties in predicting, the highly temperature dependent, lifetime of the switching elements used in those PECs. Failure of those devices are one of the most frequent causes for the down-time in power generation plants, in particular, those utilise renewable energy sources [2]. As shown in Figure 1.1, electrical systems (including PECs) are responsible for 24% of total failures faced on wind energy systems.

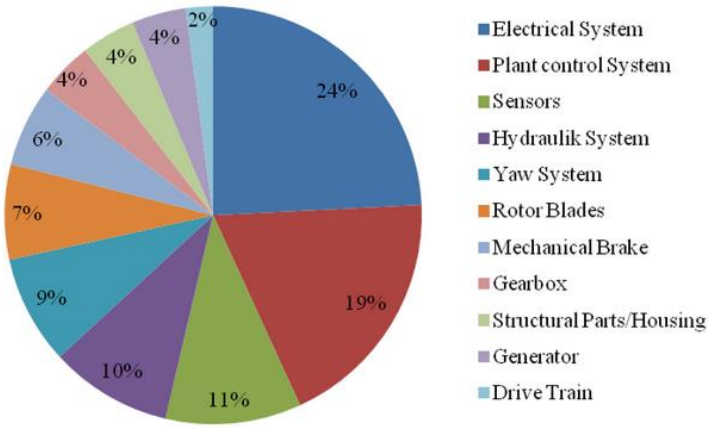


Figure 1.1 Failure rates for the wind energy system [3]

A recent wind energy update and maintenance report [4] states that 66% of PECs used in offshore wind farms is due to the break down mechanisms where the total maintenance cost is up to €300,000 per year. Furthermore, it is stated that estimated lifetime of both wind and solar energy conversion system is only 20-25 years because of the unaddressed issues, such as uncertainty of mission profiles, strength of components, lack of understanding of failure mechanisms [1],[5] and increase in the electronic content and complexity (i.e. heat coupling effect [6]). Accurate analysing of reliability of converters is crucial for preventing permanent

damages and for increasing the lifetime of wind and solar systems [1]. Therefore, motivation for new driving methods, increments in cooling capacity and improvements in material properties would lead to major improvements and they are essential for end of life enhancement.

1.2 Power Electronic Converters in Renewable Energy

Semiconductor devices are the essential components determining the efficiency of PECs for energy conditioning [7]. Some of the key switching elements used in the converters include Silicon-Controlled Rectifiers (SCR), Gate Turn Off Thyristors (GTOs), Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Transistors [8]. The Insulated Gate Bipolar Transistor, IGBT, is one of these semiconductor devices which are operated as switching elements in PECs in high switching frequency and current-voltage rating applications [9]. PECs in renewable energy systems consist of a set of combination of devices such as driver, cooling system, capacitors and power module. A view of a PEC can be seen from the Figure 1.2 [10] embedded in a wind turbine.

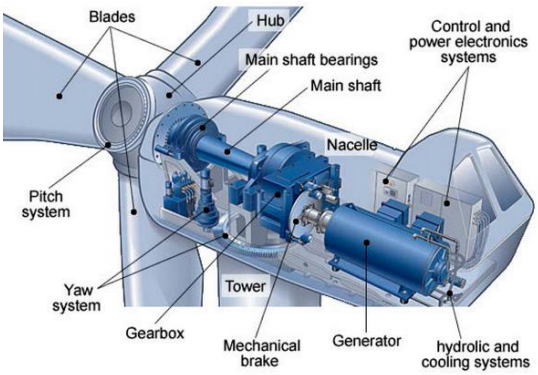


Figure 1.2 Components in Wind Turbine Hub [3][10]

PECs used in renewable energy systems can be divided into three different types, namely; DC-DC converters, DC-AC rectifiers and AC-DC inverters [11]. A voltage source DC-AC inverter linked with a DC-DC boost converter is shown in Figure 1.3.

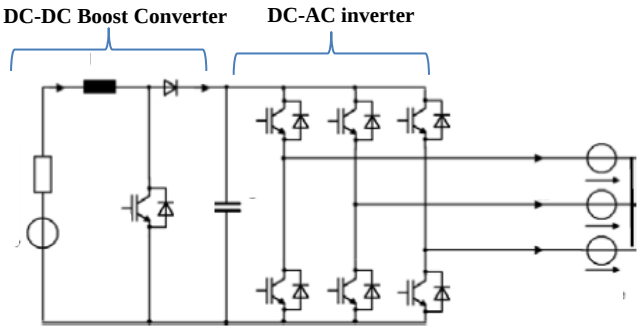


Figure 1.3 Voltage source DC-AC inverter linked with a DC-DC boost converter

1.3 Failure Mechanism of Semiconductor Devices

IGBTs have earlier break down mechanisms compared to other elements of converters [12]. This is because thermo-mechanical effects or long-term exposure to high temperatures are caused by variable mission profile [13]. IGBTs consist of different layers (see Figure 1.4) with different material properties. During its operation, heat flux transfers through different heat paths from die chip to cooling system where thermal cycling generates temperature fluctuations within these layers. Therefore, stress occurs within bonded materials with different coefficient of thermal expansions (CTEs) [14]. It causes fatigue at different locations of the power module such as bonding wire, solder and failures occur eventually [7].

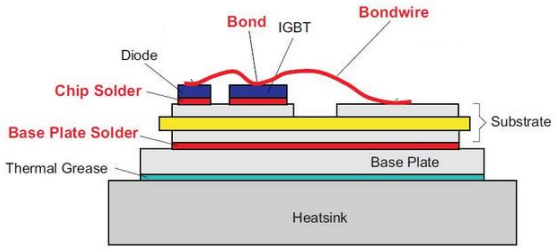


Figure 1.4 Structural Details of IGBT Module [1]

Temperature and temperature cycling are the major stressors (see Table 1.1) that affect the IGBT reliability. According to Lu et al. [15], almost 60% of failures are temperature induced as shown in Figure 1.5, and for every 10 °C temperature rise, the failure rate nearly doubles in the operating environment. In practice, operating mean junction temperature has to be between the maximum and minimum allowed ratings, specified in datasheets, which are generally less than 125°C to avoid possible faults.

Table 1.1:Failure Mechanisms of PECs [1]

Failure Mechanisms	Failure Sites	Relevant loads
Fatigue	Die attach, wire bond/TAB, solder leads, bond pads, interfaces	ΔT, DT/dt, dwell time, ΔH, ΔV
Corrosion	Metallisation	M, ΔV, T
Electro migration	Metallisation	T, J
Conductive filament formation	Between Metallisation	M, ΔV
Stress driven diffusion voiding	Metal traces	S, T
Dielectric breakdown	Dielectric Layers	V, T

T: temperature, **H:** humidity, **Δ:** cyclic range, **V:** voltage; **M:** moisture; **J:** current density; **∇:** gradient; **S:** stress

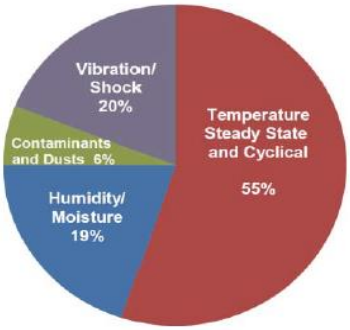


Figure 1.5 Chart of break down mechanism [16]

Two main failure mechanisms are solder fatigue and bond wire lift-off. Thermal resistance increment occurs due to the solder fatigue, and on-state voltage increment is commonly caused by the wire bond lift off [17]**.** In PECs, the failure of one component, such as DC link capacitor, may affect the operation of another one which causes over voltage stress on other switching devices and possible faults [18]. However, these components have also individual failure mechanisms which have significant impact on the reliability of PECs. For instance, Aluminium Electrolytic Capacitors (ALEC) and Metallized Polypropylene Film Capacitors (MPPFC) are used as DC-link capacitors; and high capacitance Multi-Layer Ceramic Capacitors (MLCC) are commonly used in DC-DC converters [19]. Failure mechanism comparison for the three different types of capacitors can be seen in Table 1.2. The key factor in the reliability of the electrolytic capacitors, for instance, is called Effective Series Resistance (ESR). The evaporation of electrolyte was investigated by Harada et al. [20] and linked as the indicator for lifetime of capacitor as it experiences high thermal profiles and

ages. The capacitor lifetime has considerable effect on the converter lifetime hence can be investigated in more depth as a future work but it is out of scope of this research.

Table 1.2: Failure Mechanisms comparison for capacitors [19]

Capacitor Type	ALEC	MPPFC	MLCC
Dominant failure modes	Wear out		
	open circuit	open circuit	open circuit
Dominant failure mechanisms	electrolyte, vaporization; thermo mechanical reaction	moisture corrosion; dielectric loss	insulation degradation; flex cracking
Most critical stressors	*T, V, I*	*T, V,* humidity	*T, V,* vibration
Self-heating capability	moderate	good	no

In contrast, inductors have the lowest failure rates in the lifetime of the power electric converters [21]. The failure can happen by the overheating and permanent change in the inductance and this count is for only 3% of the total failure reasons in PECs.

Power diodes cause 10% of total failures in PECs [22]. With the recent technological improvements on power modules where the diode chips are manufactured along with IGBT ones, the lifetime of the PECs depends on the cross-coupling heat mechanism among these semiconductor components. Therefore, electro-thermal behaviour of the diode chips is important for accurate estimation of lifetime of the PECs. Failures are mostly due to the variable temperature profile caused by the non-ideal doping behaviour during conduction and blocking modes of the operation when used as recovery and freewheeling diodes. As the current rating increases, even more degradation occurs between metal contacts and silicon chips [23].

1.3.1 Wire Bond Lift-Off

Reconstruction of the aluminium metallization mostly initiates bond wire lift-off due to the plastic stress relaxation of the aluminium. During power cycling, this causes increment in the collector to emitter voltage which results in higher power losses and hence increases temperature profile of chips. This expedites the bond wire lift-off due to the stress caused by thermal expansion between wire bond and the chip [24]. A sample view of the wire bond lift-off can be seen in Figure 1.6.

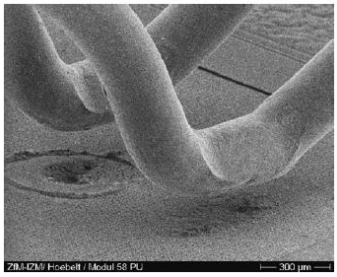


Figure 1.6 Wire bond lift off mechanism [17]

After an emitter wire lift off, the associated chip is no longer able to conduct the current; hence, other bond wires are forced to conduct higher current. This also causes a continual lift off for the other wires as they may experience more current than they are capable of [24].

1.3.2 Solder Fatigue

High temperature fluctuations affect the reliability of soldered joints by developing cracks and fatigue processes that eventually result in failure as seen from the Figure 1.7.

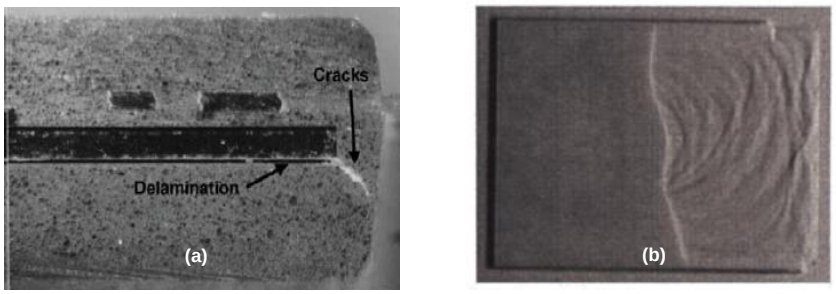
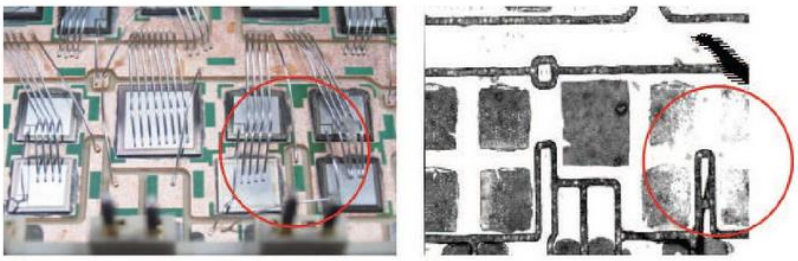


Figure 1.7 (a) Solder Fatigue and (b) Cracks and ceramic substrate failure [25] [26]

The failure occurs due to the different thermal expansion properties of the layers joint by the solder such as silicon and copper. This layer is also subjected to high shear stress leading to failure due mismatched CTE between layers and temperature gradients. Due to fatigue, this eventually grows to cracks leading to critical heat transfer reduction and hence increase in die generated heat [27]. Chip solder fatigue due to power cycling test is shown in Figure 1.8 [28].



(a) (b)

Figure 1.8 Chip Solder Fatigue caused by power cycling (a) Photograph and (b) Ultrasound Image [28]

1.3.3 Reconstruction of Metallization

This layer is made of metalized aluminium that has different thermal expansion coefficient to silicon and ultimately leads to fatigue due to temperature variations. At temperatures range higher than 175 °C diffusional creep and plastic contributions; at temperatures lower than 175 °C plastic deformation is the cause of failure mechanisms [29]. A recent research conducted by Arab et al. [30] proposed that the reconstruction occurs due to a short circuit fault. A sample reconstruction metallization can be seen in Figure 1.9 [31].

(a) (b)

Figure 1.9 (a) Optical and (b) X-ray image of a diode after power cycling test [31]

1.4 Silicon and Silicon Carbide Technologies

Thanks to recent developments, operating voltage of silicon (Si) IGBTs have reached up to 6.5 kV with 1-100 kHz switching frequency range [32],[33]. IGBT chip thickness reduction, for the purpose of improving dynamic electrical properties, causes higher thermal resistances [34],[35]. To overcome such challenges, the recent trend is moving towards different technologies such as transistors built from Silicon Carbide (SiC) and Galium Nitride (GaN) [36],[37]. Physical material specification differences among these technologies and their superior properties can be seen in Table 1.3. It has been investigated that SiC

structured transistors can be operated at higher switching frequency and temperature capacities [38],[39]. Conventional Si IGBTs can be operated at higher current densities with lower frequency while the SiC MOSFETs have better efficiency at higher switching frequencies over 100 kHz**.**

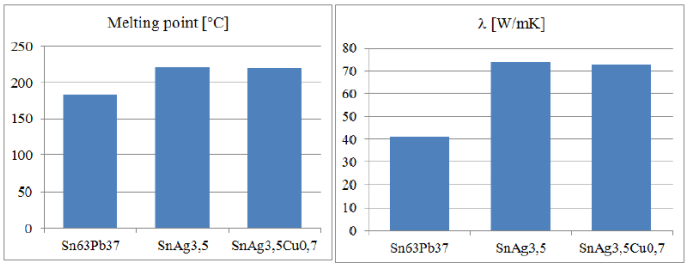
Table 1.3: Physical characteristic differences among semiconductor technologies [40]-[41]

Properties	***Si***	***GaAs***	***GaN***	***4H-SiC***	***6H-SiC***	***Unit***
Crystal Structure	Diamond	Zincblende	Hexagonal			-
Bandgap (E_G)	1.10	1.43	3.5	3.26	3	eV
Electron Mobility (μ_n)	1400	8500	1250	900	380	cm^2/V_s
Hole Mobility (μ_p)	600	400	200	100	80	cm^2/V_s
Dielectric Constant (ε_S)	11.8	12.8	9.5	10.1	9.66	-
Saturation Drift Velocity (v_s)	$1x10^7$	$2\ x10^7$	$2.7\ x10^7$	$2.7x10^7$	$2\ x10^7$	cm/s
Breakdown Field (E_B)	$0.3x10^6$	$0.4\ x10^6$	$3\ x10^6$	$3\ x10^6$	$3\ x10^6$	$V_{/}cm$
Thermal Conductivity (k)	1.5	0.5	1.3	4.9	4.9	W/cm°C
Melting Point	1420	1283	2500	2830	2830	°C

Recently developed SiC MOSFETs have much smaller channel mobility compared to conventional ones [42]**,**[43] but at higher total cost [44]. On the other hand, the thermal conductivity of SiC is much higher than that for silicon [45], so generated heat can easily be transfered from the device.

1.5 Lead Free Solder and Silver Sintering

Lead (Pb)-containing solders i.e. Sn63Pb37 have been in use in power electronic manufacturing thanks to its low cost and melting temperature along with excellent wending properties with Cu, Ag etc. However, it has been replaced with lead free type solder due to lead (Pb) inherent toxicity. After the publication of RoHS requirements in 2006, significant shift has been made towards using these Pb-free power modules. Material properties and reliability aspect of Pb-free solder have been studied in literature [46] for different application types [47] and compared with the Pb-containing solder [48]. As discussed earlier, solder is a vital material for determining reliability of the power modules hence, properties of lead free solder alloys need to be fully understood for accurate lifetime estimations. For example, the Sn–Ag–Cu solder alloy, Sn96.5Ag3Cu0.5, has low melting temperature and good wetting ability compared to Sn–Ag solder alloys. The thermal parameters of Pb-free and conventional Pb-containing solders can be seen in Figure 1.10.



(a) (b)

Figure 1.10 (a) Melting point and (b) thermal conductivity of Pb-containing and Pb-less solders[47]

On the other hand, soldering can be replaced by a recent technology called sintering, in power modules. The sintering is based on pulverised silver which forms a material connection when pressure and temperature are applied [49]. It combines two fine grained ceramic or metallic materials, usually under high pressure, at temperatures below the melting point of both materials. The sinter joint is a thin silver layer with better thermal resistance compared to the soldered joint. Due to the high melting point of silver (960 °C), less joining fatigue occurs which increases the life time and power cycling capability [49].

1.6 Reliability and Health Monitoring

Capability of the power electronic devices to fulfil expected operation under stated conditions, is defined as its reliability, in certain period of time [50]. In spite of the various studies, still there are limitations in the reliability research for power electronics. Wang et al. [1] have summarized these limitations as; lack of systematic design for reliability (DFR) approaches are over reliance on calculated value of mean time to failure and meantime between failures. Handbook based failure prediction methods [51] aim to provide statistic estimations for remaining lifetime of converters but they lack valid justification [52] since they are not function of time dependent temperature profile [53]. For instance, Military Handbook 217 [54] establishes how to predict lifetime of electronic products in terms of the factors that influence reliability. However, the methods are not function of temperature gradient or time dependent temperature profile [53]. Temperature cycling affects failure rate change with materials which are not considered in such books [1]. Therefore, accuracy of such studies would not be high. One useful approach is the physics of failure approach that is based on root caused failure mechanism analysis and the impact of materials, defects and stresses on product reliability [1], [14], [15].

1.7 About this Research

In order to derive accurate reliability analysis for PECs, it is necessary to understand the physics of their failure in terms of thermal characteristic. This research firstly investigates the effects of the operational factors such as control methods, switching algorithms, load variations, environmental effects, on the thermal profile of the power electronic devices. Then, it proposes accurate electro thermal modelling and active controlling techniques for these devices in order to decrease thermo-mechanical stress and temperature variations on layers made of different material used in conventional power modules. This section outlines the specific research direction. Based on the motivation of the work, originality and limitation of the research are also addressed.

1.7.1 Contribution to Knowledge

1. An electro thermal model was implemented, which is applicable not only for discrete but also for continuous temperature monitoring of integrated switching devices, using Simulink and embedded within real time dSPACE environment.
2. In an attempt for the replacement of expensive thermal imaging procedures, Finite Element (FE) models for topologically different Si IGBTs and SiC MOSFET were derived with COMSOL which take real-time power losses as input and produce heat distribution over the devices.
3. A new variable DC link and switching frequency control method, within the PWM driving strategy of a two level back to back converter, which is coupled with a wind energy system, was implemented for stress/strain and power cycling reduction.
4. For the first time in literature, the effect of the different maximum power point algorithms (MPPTs) on the reliability of the power electric converters used in PV system was investigated. Previous studies only dealt with comparison among the MPPTs efficiency, accuracy, tracking speed etc.
5. An experimental, electro thermal monitoring for a physical three-phase IGBT inverter power module was implemented for temperature and lifetime estimations. Suitability of the system was tested by a physical wind turbine test rig under different operating conditions and verified with model based results.

1.7.2 Aim and Objectives

1.7.2.1 Aim

The aim of this research is to investigate the effects of the environmental and operating conditions on the electro thermal performance and reliability of the power electronic converters embedded within renewable energy systems. Based on this, the research considered deriving real time electro thermal modelling, new control strategies, and reliability models to decrease thermal stress and to enhance the lifetime of related devices.

1.7.2.2 Objectives

1. To review the research status in the electro thermal modelling, operating conditions, physical material properties and reliability of insulated gate bipolar transistors operated in power electronic converters of renewable energy systems.
2. To derive accurate electro thermal and thermo mechanical FE models for the semiconductor switching and power electronic devices used in renewable energy systems.
3. To investigate electro thermal characteristics of topologically different semiconductor switching devices based on their physical and operational differences.
4. To derive thermo mechanical FE models for power electronic devices used in renewable energy systems.
5. To derive reliability models for semiconductor switching devices as a function of electro thermal and thermo mechanical characteristic.
6. To implement Simulink models of wind and PV systems with embedded power electronic converters and their associated control algorithms to decrease the thermal stress and enhance the lifetime during variable environmental conditions.

1.8 Structure of Remaining Chapters

The remaining chapters of the thesis are organised as follows:

Chapter 2 presents the literature survey of the project. Current research status in electro thermal and thermo mechanical modelling of the power electronic converters, their material type developments and control technologies as well as reliability and lifetime analysis are reviewed. Suitable technologies and knowledge are highlighted for the design of novel control algorithms which is needed to enhance their end of life.

In Chapter 3, implementation of an electro thermal model for a multichip single IGBT power module is presented with theoretical approaches of thermal stress analysis. The model was built by using COMSOL finite element package and then implemented in Simulink package based on the complex heat interactions and coupling effect across IGBT chips. This chapter also presents implementation of real-time electro thermal model and detailed investigations into the performance of trench gate Punch through (PT), non-Punch through (NPT), Field Stop (FSTP) IGBT and SiC MOSFET topologies. They are firstly modelled using 3-D multi-physics FE modelling to gain clear understanding of their thermal behaviour. Subsequently, modelling outcomes are verified by using those devices as switching elements in operational boost converters.

Chapter 4 critically studies the thermo mechanical modelling and the effects of thermal stress on the reliability of power electronic converters. By considering the variations in wind characteristics, a mitigating technique is offered by first, developing realistic Full Scale (FS) and Partial Scale (PS) induction generator models combined with a two level back-to-back PECs. Subsequently, a switching algorithm was derived which reduces PEC's operating temperature by controlling its switching patterns. The experimental validation for the thermal stress mitigating technique of a three phase DC-AC inverter module used in a wind system is presented.

Chapter 5 studies lifetime reliability analysis for power electronic devices based on the electro thermal and thermo mechanical characteristics. The model is validated via dSPACE real time implementation with a physical permanent magnet generator based wind turbine system test rig. It also investigates the effects of maximum power point tracking algorithms on lifetime and thermal stresses in DC-DC converters under different operating conditions.

Converter's electro thermal characteristics were firstly modelled. Subsequently, experiments on photovoltaic solar system were carried out using two different MPPT algorithms, namely, perturb and observe (P&O) and incremental conductance (IC).

Achievements, conclusions and future work are depicted in final chapter.

Chapter 2

Literature Review

2.1 Overview

This chapter presents the literature survey of the project. The review process includes electro thermal, thermo mechanical modelling and lifetime analysis of semiconductor switching elements, specifically their material properties and reliability in power electronic converters embedded in wind and solar energy applications. At the end of the literature review, the research synthesis and main direction of the project are outlined.

2.2 Electro Thermal Modelling

Electro thermal models are consist of thermal and power loss models, which can continuously monitor temperature variation for a device in power electronics. Heat distribution through the power electronic devices are due to the power loss occurring which causes the temperature to increase. Coupled temperature depended power loss and thermal models are implemented to monitor thermal profile of power electronic devices.

2.2.1 Thermal Modelling

Thermal models aim to describe transient thermal behaviour (transient thermal impedance) of power electronic devices or converters to estimate mean and varied temperature profiles under operation. Thermal modelling techniques are based on two main forms of reactance theorems defined by Foster [55] and Cauer [56]. Foster [57] also improved the modelling approach based on earlier defined models with thermal RC elements. Until late 90s, the improvements were continued by using 3-D finite element modelling analysis. The accuracy of such a model is high since the applied equation to a finite boundary condition is solved for small parts of a material in scaled elements. At present, however, these simulations require long transient thermal simulations for power electronic applications [58]. Another approach can be the usage of analytical Fourier series so that the extraction of RC thermal equivalent circuit can be avoided [59].

2.2.1.1 Finite Element based Thermal Modelling

Finite Element Modelling (FEM) was first developed in 1943 by R. Courant, who utilized the Ritz method of numerical analysis and minimization of variational calculus to obtain approximate solutions to vibration systems [60]. Initial finite element forms of Poisson's equation and the electron and hole current continuity equations are derived by Barnes and Lomax [61] with implementation of fourth order (Hermite bicubic elements) methods. First thermal studies are based on the work proposed by Hsu and Vu-Ouoc [62] that accomplished heat transfer simulations by a rational approach. Construction of thermal circuit networks of the heat equation by the finite element method with FLOTHERM simulator was accomplished with triangular and rectangular elements in the 2-D, and tetrahedral and cube elements in the 3-D case. Hefner and Blackburn [63] proposed a model which solves dynamic electro thermal behaviour of power electronic systems. However, this model was disadvantageous since it can only predict the junction temperature and is unable to solve exact heat distribution through each layer.

Székely [64] developed a model with THERMODEL software to describe heat conduction of three-dimensional physical structures. The simulation based time-constant spectrum was related both with the time and frequency responses. The relation was solved based on a complex convolution method that uses the Fourier-domain inverse filtering method. Bagnoli [65] studied a model for implementing an equivalent thermal circuit of an electronic device by infinite and convergent series of time constants. More practical approach was proposed by Rencz et al. [66] where an algorithm collects the junction temperature estimation under transient operation and updates the compact RC models for a semiconductor device using frequency domain analysis.

2.2.1.2 Analytical and Finite Element based Thermal Modelling

The approaches discussed above are all employ resistor capacitor networks as thermal equivalent circuits. Although, they can be accepted as computationally fast, they cannot represent actual 3D heat diffusion path through the devices. For instance, transient thermal identity extraction based study, assessed by Ciappa et al. [67] with Foster equivalent circuit,

was unable to represent actual heat path and lateral heat spreading effect that occurs if the silicon layer (where the heat is generated) is smaller than the cross section of the conducting material.

Christiaens et al. [68] proposed a methodology that represents dynamic thermal model of chip packages by using analytical Fast Fourier Transform technique. The model includes compact resistor-capacitor network that predicts the dynamic junction temperature response under any arbitrary set of external cooling conditions.

More accurate thermal models were derived by Masana [69] who proposed analytical solutions to heat spread angle estimations by taking the chip and substrate dimensions into account and changing angle accordingly. The methodology showed good accuracy compared to the Fourier series based thermal model analysis with the 10% of theoretical exact solutions of infinite series techniques. Culham et al. [59] proposed an analytical approach for thermal characterizing based on the steady-state solution of the Laplace equation for rectangular geometrical chips. Three dimensional Fourier series were applied to solve the conduction law within each layer of the package. The validation between published experimental data showed 5% increased accuracy compared to the traditional procedures proposed by Christiaens et al. [68].

Masana extended the previously developed models [69] by 3-D analysis in [70]**.** Each thermal resistance and capacitance pairs were used as input to an electric circuit simulator to obtain the transient response of the package. The results showed good accuracy compared to the FE model with ANSYS, however the employed methodology is still unable to solve exact solution to heat transfer equation and characterise the coupling effect [6] between internal layers of any power electronic device. Janicki et al. [71] proposed an analytical solution of the three dimensional heat equation with the using Green's functions. The results of transient thermal simulations of a real hybrid power module are compared with infrared measurements. The derivation was validated with accurate set of data; however it showed complexity and difficulties to be modelled with any circuit simulator software. Vermeersch and Mey [72] developed an extension of complex thermal impedance in phasor notation. Heat dissipation was studied as a square source that spread through the device under a fixed angle. The temperature distribution was generated by integrating the Green's function over the source area. The approximated relative error was observed as less

than 6%; however the analytical solution was only valid when the heat sink temperature was fixed and equal to zero. Swan et al. [73] implemented an analytical thermal model for a power device module in MATLAB/Simulink with block diagrams. A Fourier-based solution was used to solve the heat equation in 1-D & 2-D. The model was validated against FEM simulations with FLOTHERM. The 1-D model showed 3% where the 2-D model showed 4% difference for peak temperature rise for each model.

2.2.1.3 Boundary Condition Depended Finite Element based Thermal Modelling

Augustin and Hauck [74] proposed a new method for the generation of boundary condition dependent dynamic thermal compact models by state space modelling by transforming the state space model into a Kirchhoffian network. However, presence of the introduced Lagrange polynomials increased the complexity simulations even though good accuracy was obtained between the results and FE model with ANSYS. Darwish [75] proposed an addition analytical solution to Masana's model [70] that derives an exponential approximation for thermal resistance calculation, based on Fourier's conduction law. The theoretical solution was verified with FE simulations with ANSYS. The accuracy was improved up to 1-2% between FEM and analytical solution, compared to Masana's [70] method.

Kiffe and Wachutka [76] proposed a thermal model consists of a set of Foster-type thermal equivalent circuits. The modelling and measurements consisted of only one single chip analysis and the approach could not be extended for multichip devices [77]. Schweitzer et al. [78] also showed numerical effects during the calculation of the structure function and 3D heat spreading effects on determining the junction to case thermal resistance. The derived structure function showed around 5-15% uncertainty with FE modelling results.

Hocine et al. [79] studied thermal analysis of a IGBT module by using MSC.NASTRAN. The junction temperature for an input heat power located as hot spots; however, the results consisted of self-heating phenomena in the device only. Stupar et al. [80] proposed a model to estimate junction to case and case to heat sink thermal resistances, experimental tests were performed when the device is attached to a cold plate. The validation of the estimation was assessed based on the information supplied in datasheet and with GECKO CIRCUITS software; however it still had the shortage of defining thermal coupling effects.

Transient thermal behaviour of a power module was improved by Hensler et al. [81] with respect to the material properties and dimensions of the device where the thermal spreading angle is accepted as 45°. Although the analysis showed moderate accuracy (~11%) compared to the experimental estimations, the actual heat flow path was fairly investigated. Gradinger and Riedel [82] recently provided a time-variant cooling by ICE-Pack FE software. Evaluations showed that Cauer networks responded physically meaningful while the Foster networks reacted too quickly in terms of thermal resistance derivations.

Skuriat and Johnson [83] studied a comparative model between three cooling methods to extract thermal parameters for IGBT based half bridge converter [84]. This work proved that heat spreading effect can still be estimated accurately once it was compared with FE model of whole module. Azoui et al. [85] proposed a new approach for 3-D FEM which contains several cooling surfaces, and the represented non-linear properties of materials for structure of generated models. Variable thermal resistances and capacitances were used to improve heat flux estimations and results from the dynamic compact thermal model (DCTM) were found within 3% against the FEM results. Schweitzer [86] also aimed to analyse two measurement techniques, that were constant, and floating case temperature methods. The junction to case thermal characteristic difference between two methods was obtained as 15% where it was up to 31% with 3-D thermal simulation.

On the other hand, thermal models of power modules with multichip designs were proposed by Luo et al. [87] for multichip device. The thermal parameters were extracted from the experimental data and the accuracy of the model was verified by 3D FEM method simulations with ANSYS. However the thermal coupling between the chips has not been considered that it leads inaccuracy at temperature estimations. Castellazzi et al. [77] proposed an extensive experimental thermal characterization of multi-chip IGBT-modules. Proposed technique showed comprehensive and flexible simulation results since they were based on Cauer-T Thermal model and interconnects to parasitic elements of IGBT. Yu et al. [88] proposed an approach which predicts individual self-heating temperatures by superposition to calculate the heat spreading. Poller et al. [6] modelled the substrate of a standard IGBT power module with ANSYS. It was discussed that with increasing frequencies, the cross coupling effects cannot be reproduced correctly and it was the main cause of inaccuracies.

Proper thermal models with heat coupling effect analysis were considered by Drofenik and Kolar [89]. The proposed method derived in terms of convection cooling (forced air model with computational fluid dynamics, CFD), thermal hotspots on the heat sink base plate, thermal time constants of the heat sink, and thermal coupling between different power modules mounted onto the heat sink. The work studied a thermal impedance matrix that was convenient for thermal coupling effect estimations and most suitable way to represent actual heat path through the device. The experimental results also showed better accuracy of the heat sink model with temperature errors below 10%. Drofenik et al. [90] expanded the study proposed in [89] from air cooled to a water cooled heat sink model for a 3300V/1200A power module. A dynamic thermal model that consists of the mutual thermal coupling of neighbouring dies was modelled for integration into a circuit simulator. In this case, FEM results were compared with an infrared temperature measurement set of data. Thermal impedance matrix was expanded for a total of 36 chips heat source and 3-D geometry was implemented with a boundary condition of convection heat flux that represents a water cooled heat sink where water circulated inside the pumps. Hot spots detected in wide range of surface at specified locations on module and material properties were taken as temperature dependent as variable arguments. 2% of maximum temperature difference was observed when compared between FEM and infrared camera estimations.

2.2.2 Power Loss Modelling

Power losses occur due to the rapid changes in current and voltage ratings and they generate heat over the devices. Power Loss models can be implemented in different ways. Since energy losses are accepted as the main cause of the heat generation through power semiconductor devices [16], modelling a power loss model that represents the actual behaviour (designing switching and conduction duration accurately) of a device is essential for a proper electro thermal model.

Blinov et al. [91] studied improvement of conventional power loss calculation methods by using manufacturers' datasheet parameters. Energy losses supplied in datasheets were fitted by curve fitting methods with third order exponential functions. Each loss was calculated with respect to the sample current-voltage input characteristics. An analytical

method of estimating losses was also derived by parasitic components of the device and compared with fitted curves. Good approximation was assessed with such technique but the order of polynomial causes miscalculations in high frequency operation. Similar model was proposed by Rui et al. [92] with the extension of temperature and on time resistance dependent loss estimations. The simulation was executed with PSCAD/EMTPC software and 1.4% loss rating was estimated compared to the analytical calculation. The model cannot be easily expanded with a thermal model although the accuracy was quite high. A quite similar approach was also followed by Ivakhno et al. [93]; however the model was implemented with Matlab/Simulink blocks. With the help of the logic blocks in Simulink, power loss calculation was acquired based on the output current and voltage signals of IGBT/Diode block element, available in SimPower library. Acceptable accuracy of dynamic loss calculation (<10%) was achieved under hard switching. Different modulation strategies (i.e. SPWM, THIPWM, SVM) and their effect on power loss estimations were also studied by Santos and Antunes [34] for three level neutral point clamped converter (3L-NPCC). Comparison between two and three level converters power loss analysis were also presented by Orfanoudakis et al.[94] where three level application showed better performance in high switching operations. Radan [95] studied effects of the losses on DC link capacitor. Intensive studies have been performed on carrier-based, sinusoidal, space vector and sigma delta PWM methods in open loop control of inverters [96]. It was proven that the selection of topology and control techniques may vary according to power demands of inverter.

Zhou et al. [97] studied an electro thermal model that was relatively applicable for reliability analysis. The main purpose of this work was to improve accuracy of power loss model by designing a compact electro thermal model whilst keeping the simulation time step relatively large (i.e. in the order of milliseconds). The proposed look up table based simulation method was more promising for life time analysis since it is computationally more efficient compared to model studied in [58]. Another electro thermal model for an inverter consists of six IGBTs in PLECS was proposed by Huang et al. [98]. Although the model was computationally efficient for accurate power loss calculation, it lacks of implementing heat path through the device and it was only capable of junction temperature

estimations. Moreover, the model cannot be extended for reliability analysis although it was suitable for wind power converter application where the frequency was variable.

Ma and Blaabjerg [99] also studied and extended the electro thermal model developed in [98] from 2L-BTBC to 3L-NPTC. The proposed simulations were carried out based on PLECS blockset in Simulink. Look up table based power loss calculations were integrated into thermal models based on the datasheet supplied by the manufacturer. Unfortunately, this model also had the disadvantage of inaccurate temperature estimation among physical layers and it was not compatible with reliability modelling, as well. Ma et al. [100] developed a case study among three-level and five-level H-bridge and neutral point clamped topologies in terms of electro thermal performance based on the developed models in [101]. Simulink based modelling approach was applied. It was estimated that three levels neutral point clamped converter has better electro thermal performance among other topologies; therefore, it is more reliable under same conditions (i.e. power cycling and PWM strategy) according to this particular study. Another electro thermal model was developed by Pittini et al. [102] for a 2L-BTBC converter with PSCAD block sets. The thermal and energy loss parameters were obtained from the device datasheet. Although the software leads user friendly implementation, the physical user interface was not capable of electro thermal modelling of multichip design power modules and reliability analysis.

A recent promising study was implemented by Ma and Blaabjerg [14] to extract the chip number from an IGBT module. It aimed to calculate the chip numbers *N* according to the module's conduction voltage at a certain load current *Iload*. Since the load current is equally distributed because of the parallel connection, the conduction voltage is equal for all chips where the chip load current is *Iload/N.* This proposed analytical method can be accepted as accurate since the internal resistance of the IGBT/Diode Modules is equal for each chip and unlike the other proposed models discussed until now; it is quite convenient for calculating temperature distribution through each chip over the module. Similar methodology was also implemented by Wigger and Eckel [103] earlier for proper scaling of single chip measurements to module-level. Ma et al. [104] recently developed complete power loss and thermal model in terms of device rating as input variables for multichip power modules.

2.3 Thermo Mechanical Modelling

2.3.1 Temperature and Power Cycling

As mentioned earlier, solder joints of different layers are one of the weakest points of power electronic devices; hence, they have great impact on overall reliability of PECs. Mi et al. [105] proposed a reliability study for lead-free solder joints using Weibull distribution based on an accelerated life test. Thermal cycling test was applied and number of cycles to failure was predicted by a new censored data processing method. It was investigated that occurred fatigue in lead-free solder joint under thermal is creep fractured and the crack initiation always occurs at the interface of solder and copper layer. Feller et al. [106] also proposed a study for investigating the effects of raising the maximum operating temperature of IGBT modules and the required design modifications of solder materials. Two solder materials, namely Pb40Sn60 and lead free Sn96.0Ag2.5Bi1Cu0.5 were experimentally compared by creeping tests. They also stated that joint fracture mechanism can differ a lot between different solder materials which lead to a different fracture surface. They offered that for a higher operating temperature; the lead-free solder can be chosen carefully since evolution during power and temperature cycling to meet the reliability requirements should be further investigated. Ji et al. [107] proposed a novel design to consider die-attachment solder failures induced by short power cycling and baseplate solder fatigue induced by the thermal cycling. The work aimed to minimize the total thermal resistance and the plastic work accumulated in the solder layer through equation transformation in FE modelling. It has been concluded that different optimization characteristics were needed for power and temperature cycling operations for calculating thermal resistance effectively. Based on this, Bouarroudj [108] proposed a comparative thermomechanical stress study by using Finite Element simulations for power and temperature cycling conditions 600V-200A six-pack IGBT power modules in automotive applications. For the power cycling test condition gate threshold voltage shift and solder cracks were observed at the junction temperature of 60°C with an ambient temperature of 90°C. However, for the thermal cycling test caused only solder deformation at the temperature cycling range of -40°C to 120°C. The study concluded that power cycle at low temperature is almost as destructive as a thermal cycle for solder lifetime and those chips

are subjected to very high compressive stresses especially at low temperature levels. In order to understand the solder joints degradations and stress–strain distribution at the solder joints under cyclic thermal loading, a multi-layered IGBT module was analysed in [27] with the ANSYS FE software. Since the solders are highly viscoelastic in nature, a nonlinear viscoplastic material was used for solder in the analysis defined by Anand's constitutive model [109] while other layers were considered to be elastic. This model was also studied by Wang et al. [110] to represent the inelastic deformation behaviour for solders such as 62Sn36Pb2Ag, 60Sn40Pb, 96.5Sn3.5Ag, and 97.5Pb2.5Sn. Anand's model was successful for representing the inelastic deformation behaviour of solders at high homologous temperature and is promising for FE modelling studies for deriving the stress/strain responses of wide range of solders. For deriving solder joint reliability during thermal cycling, Motalab et al. [111] developed a new reliability prediction procedure that also contains constitutive and aging effects. An improved Anand's viscoplastic model was studied by considering includes material parameters. Using the measured fatigue data, solder fatigue failure criterion was derived by Coffin-Manson (strain-based) and Morrow-Darveaux (dissipated energy based) type fatigue criteria. It was expressed that the associated fatigue models for solder joints are affected by isothermal aging prior to cycling.

2.3.2 Warpage

Solder layer bumps due to warpage of a semiconductor power electronic device in its operation. Warpage can be defined as a distortion where the surfaces of the moulded part do not follow the intended design shape. Zhou et al. [112] recently investigated warpage and residual stresses induced by reflow process for a 1200V IGBT module by FE and experimental studies for substrate and copper layers. Viscoplastic behaviour of solder was also considered for predicting warpage and thermal stress, accurately. It was proposed that increasing the thickness of the alumina layer maximizes both warpage of the module and residual stress. Also, the increment of the copper substrate would lead deductions of the warpage; however, this would increase the residual stress. Based on their experimental study, little influence on deformation magnitude and residual stress was obtained by the pre-warpage process.

Another investigation for lead free Sn96.5Ag3Cu0.5 solder behaviour was presented in [55] in terms of strain rate at different temperatures and tensile speeds. It was found that both

temperature and strain rates have crucial effects on tensile and creep properties. Compared to the Pb-containing solders, lead free solder has lower stress of 20 MPa at room temperature and revealed certain creep resistance, resulting in a long time of creep fracture. Also, compared to the Pb-containing Sn63Pb37, flat plastic range of this lead-free solder had better deformation resistance.

Thermo-mechanical performance of a microchannel-based technology within an actively cooled 1200V 75A IGBT module was investigated by Xu et al. [113] and its performance was compared with normal operation by finite element analysis. Residual stress caused by reflow soldering process and operating stress considering the residual stress in previous process were studied as well as the plastic behaviour of soft solder and copper. It was investigated that the chip temperature could be reduced up to 80 °C by the usage of copper microchannel baseplate. Residual stress of the module caused by CTE would cause more than 1500 mm warpage and it also bends the silicon chips with a stress of 57.3 MPa on bottom and 188.2 on the top of the layer. Based on the optimisation study, copper thickness layers were suggested to be increased up to 3 mm where the thermal interface material thickness needs to be 0.2 mm.

2.3.3 Sintering

As mentioned earlier, sintering is based on pulverised silver which forms a material connection when pressure and temperature are applied. Dudek et al. [114] studied the thermo-mechanical reliability design requirements of the sintered silver layers for IGBT devices by FEM. By using a micromechanical cell model, shear loadings with in-situ deformation were analysed for monitoring the silver behaviour during passive and active thermal cycling. It was observed that active power cycling can induce failure modes different from passive cycling. For instance, maximum principal stress in the die increases with active heating and as the cyclic inelastic strain in the Ag sinter layer is regarded, it gets very low dependent on the Ag material properties. Therefore, no simple solution was presented for thermo-mechanical stress due to the strong interaction of various design- and material parameters; however the FE model showed good performance for future reliability prognostics of sintered devices.

Braunwarth et al. [115] further compared the soldering and sintering as die-attach technologies by using life cycle assessment for IGBT power modules. They claimed that

sinter layers can be useful since they reduce the maintenance efforts by increasing reliability unless the power module fails earlier due to other mechanism such as bond wire lift-off.

Reliability of sintered joints and soldered SAC305 joints were compared by Chen et al. [116] using cyclic shearing tests at different temperatures in terms of temperature, mean stress, and stress amplitude. The fatigue of sintered joint was found as much longer than that of soldered SAC305 one under the same loading conditions. Hence, it was concluded that sintered nanosilver joint has demonstrated a longer lifetime and better response than SAC305 joint, especially at high temperatures.

Rajaguru et al. [117] proposed a thermo-mechanical reliability finite element model for sintered silver structure of a power electronic module based on the computational approach and reduced order modelling in order to capture the strain distribution. The model was demonstrated on sintered silver interconnect between silicon carbide chip and copper substrate in a power electronic module.

2.3.4 Wire-bond

Another experimental power cycling test proposed by Forest et al. [118] studied for ageing of IGBT power modules by monitoring device temperature and on-state voltage for detecting possible wire bond degradation and emitter metallization for the test devices IGBT modules with one inverter leg and 600 V–200 A trench gate chips. These two characteristics were monitored by first implementing temperature variations induced by Pulse Width Modulation (PWM) operation in an inverter bridge built with two samples. Then, an automated measurement system was implemented for avoiding any data loss during on-state voltage monitoring. The technique showed good accuracy verified by several dozen of test devices. The average lifetime of the devices varied between 550,000 to 660,000 cycles and degradations were observed for the wire bond.

Nagl et el. [119] studied different operating conditions of a typical 1700V / 800A traction high-power IGBT module such as normal operation, short circuit with medium inductive load, and short circuit with low inductive load for identifying its power loss, temperature distributions and mechanical stress/strain distributions in a typical package by using the finite element method. Von Mises stress and strain distributions due to thermal expansion were calculated under quasi-static and pulse load conditions. It was proposed that any operation of the device causes different stresses which are the reason of thermomechanical

fatigue. It was found that average load during a normal operation is 400W where this increases up 5MW for the short circuit operations. Von Mises stress for normal operation was estimated the highest at the centre upper solder and gate bond wire.

An application based research was proposed by Paul et al. [120] for verifying importance and limitations of parameters used together within reliability tests and field applications of IGBT power modules. FE and analytical model based studies were used for simplifying the laboratory based drive cycle stress test. Compared to the application based lifetime calculation which was approximately 14095, model based cycles to failure were found as 12500 while the cycle time step was 900 seconds. The reason of stress in solder was found as power cycling operation compared to the temperature cycling. Spatial stress distribution was mainly observed at the centre of the chip where the peeling stress was close to the chip edges. This peeling stress was defined as reasonable for the delamination of system solder. The stress relaxation began at 1-2 seconds interval and the dependence of creep strain saturated after 60 seconds. On the other hand, wire bond stress was mostly caused by thermal cycling.

Medjahed et al. [121] studied wire bond behaviour on the IGBTs by applying direct current flow within the wire to reproduce the thermal cycling test used in reliability studies within FE analysis and verified the results by experimental temperature measurement. Von-Mises stress was obtained by FEM and thermo-mechanical results were compared with a 1D simplified thermal model. Both electromagnetic force and the mechanical stress were considered in numerical modelling. Bond angle amplitude was studied for current levels 5-15 A and optimized values were extracted based on the Von-Mises stress distribution. It was also concluded that the electromagnetic effects are not relevant for mechanical stress.

Another life assessment study was proposed by Chen et al. [122] for predicting wire bond life by finite element IGBT models by ANSYS. Power cycling test was conducted for life cycle data estimation and the statistical analysis was validated by these tests compared to FE model. Compared to the previous studies in literature, an additional electrical resistance at the wire bond was discovered from testing and evaluated by thermal simulation and has significant impact on the wire bond life. Bond fails were also estimated around the chip centre and expands to the edges.

Recently, Medjahed et al. [123] studied electro thermal stress for wire bonds of 1500A, 3300V, IGBT module with active current cycle under steady and transient current states using ABAQUS FE package. The maximal value (10 MPa) was located at the tail of the wire, near heel area where main failure modes occur close to this specific region. One main outcome of this study was that an AC current waveform does not produce exactly the same temperature dispatching and values as DC one.

Bielen et al. [124] described power cycling experiments using the Joule heating of the bond wires for finding failures. This was managed by varying bond wire settings to create different amounts of initial damage as introduced by the plastic deformation of the heel and the wedge. FE model was employed using ANSYS solver to calculate the stress amplitude in the heel of the bond wire in the experiments as function of current, pulse time and loop shape. The model succeeded for detecting plastic deformations around microscopic defects by averaging Von Mises stress over the wire diameter. In order to predict the expected lifetime, measured failure times (N_f) and calculated stress amplitude (S) the durability (S-N curves) were used for deriving different amounts of initial damage. Ozkol et al. [125] studied power cycling performance of IGBT modules by implementing wire bond layout of the emitter contact using electrical and thermomechanical FE analysis and experimental results. Based on the current distribution and induced mechanical stress, a new HiPak IGBT power module was designed.

2.4 Lifetime Analysis and Reliability of Power Electronic Devices

Lifetime prediction can also be assessed by well-designed compact transient thermal models [98]. This can be achieved by estimation of the damage accumulation due to thermo-mechanical stress cycling once a transient electro thermal model is coupled with [7].

Deriving accurate reliability prediction models are challenging due to the several reasons discussed in introduction and thermo-mechanical modelling sections. High reliability requirements and the lack of component manufacturer data also increase the concern on such studies. Empirical and statistical data based models showed high inaccuracies [126]; hence, physics of failure approaches need to be investigated further by considering individual material properties and failure mechanisms of power module layer and interactions among themselves during power and thermal cycling.

Zhou et al. [127] proposed a novel method for reliability improvement of a full bridge, single phase inverter system by using a dual loop controller which includes temperature control and electric power control loops. The method aimed to adjust the carrier frequency of the driving signals. Digital implementation of field programmable gate array (FPGA) board based was used for verification and number of cycles to failure has been largely increased. IGBT chip temperature was decreased from 9°C to 0.5°C based on the proposed model. Different failure mechanisms accelerated by temperature and voltage of semiconductor device were studied by Qin and Bernstein [128] such as hot carrier injection (HCI), time dependent dielectric breakdown (TDDB) and negative bias temperature instability (NBTI). It was noticed that the activation energy and voltage acceleration parameter depend on stress temperature and voltage. Two new considerations were studied: first, a modified version of the Arrhenius model to model the temperature dependence of device lifetime at given voltage; second, a modified exponential model to model the voltage dependence of device lifetime at given temperature.

Wang et al. [1] proposed a reliability and end of life study for a 2.3 MW wind power electronic converter. Selection of two power modules; namely 1.6 kA 1 kV IGBTs parallel and single 2.4 kA 1 kV IGBT were tested for their reliability aspects. It was investigated that the design principle mission profile and the topology of an individual device has a crucial effect of the overall reliability

Arifujjaman [129] presented reliability analysis of the power electronic converters for grid-connected permanent magnet generator-based 1.5 kW wind energy conversion system based on the semiconductor power losses. Different power electronic converter topologies namely intermediate boost converter, the intermediate buck-boost converter, the back-to-back converter and the matrix converter were investigated. The main target of the study was to specify which power electronic converter yields the highest mean time between failures (MTBF) and reliability in terms of power losses under different wind speed operations. It was expressed that the efficiency and MTBF ($4x10^4$ h) of the intermediate boost converter was higher compared to other topologies. The most reliable device was found as rectifier while the least reliable one was the inverter ($1.7x10^4$ h).

Isidori et al. [130] proposed another comparative reliability study for a 3L-NPCC for a 10 MW wind turbine equipped with a Permanent Magnet Synchronous Generator for five

different pulse width modulation drive methods. Simulink and PLECS simulation platforms were used to derive different modulation strategies namely sinusoidal pulse width modulation (SPWM) [131], optimal zero sequence injection [132], alternative zero sequence injection [133], conventional 60◦ discontinuous PWM and Alternative 60◦ Discontinuous PWM [134]. Among these five control methods, the Conventional 60◦ Discontinuous PWM showed the best thermal performance and the highest number of cycles for both the generator and the grid side converters. It was also concluded that the increment in the wind speed profile causes larger dispersion for the mean and fluctuation temperatures; hence, cycle lifetime of the converter largely decreases.

Xie et al. [135] proposed new failure models for power electronic converters used for 2 MW wind turbines which consider the effects of the wind speeds by using multistate probability analysis method. The wind speed data was taken from Lauwersoog and Valkenburg wind sites in Holland. It was mentioned that the failure rate and wind speed curve are similar to those between the generator output power and wind speed and confirmed that wind speeds have significant impacts on converter reliability performance. The failure probability of the converters under the rated wind speed was 95% within one year, where this is 20% for the wind speed at the Valkenburg site and 37% at the Lauwersoog site. Also, as the rated speed gets smaller, larger failure rate for converters were investigated; however the effect of cut-in and cut-out wind speeds on the failure rate of WTPCS were very small.

Wagenitz et al. [136] designed a power cycling test bench for the lifetime analysis and reliability management system of IGBT power modules converters for 1.5MW doubly-fed induction generators used in wind turbines. The test bench offered accelerated ageing of the power semiconductor devices under real load conditions with the phase legs operating at 1070 V dc-link voltage and allowing sinusoidal load currents up to 560A, at load frequencies from 0.1Hz to 13Hz with offering programmable load profiles. Temperature data is generated continuously according to the implemented load profile and software and hardware modelling was developed for online thermal monitoring.

In order to verify theoretical load-profiles with data from the field applications, Denk et al. [137] proposed a concept to record all junction temperature cycles of an IGBT power module during its operation in a test vehicle. The recorded load of test vehicles was used to predict lifetime of IGBT power modules. A modified gate driver was used to determine the

temperature sensitive IGBT internal gate resistor by superimposing the negative gate voltage with a high-frequency identification signal. Then, an online version of the Rainflow Algorithm, which relates stress reversal cycles to streams of rainwater flowing derived by Matsuishi and Endo [138], was developed for temperature cycles calculation and this enabled real-time temperature measurement for an inverter.

Arifujjaman et al. [139] presented a reliability analysis of the power electronic converters of both the permanent magnet generator (PMG) and wound rotor induction generator (WRIG)-based small wind turbine generation systems. The PMG system included a rectifier, boost converter and a grid-side inverter while the later had a rectifier, a chopper and an external resistor in the rotor side with the stator directly connected to the grid. It was investigated that the failure rate for the PMG-based power electronic converter system was 1.9009×10^{-5} and the MTBF was 5.2607×10^{4} hours (≈6 years) where the failure rate for the WRIG based system was 9.3768×10^{-6} and MTBF was 1.0665×10^{5} hours (≈12 years). In other words, the PCS of the WRIG based power electronic converter system illustrates higher reliability than the PMG based system.

Another reliability study, was proposed by Kostandyan and Ma [18] for crack propagation failure mechanism of solders of a 1700 V and 3600 A IGBT power module manufactured with 24 parallel connected IGBT chips used in a 2.3MW wind turbine. First, order reliability method was used to define failure of each chip defined as 20% shrinkage of the total solder interconnected area under the chip, which defines crack length of 0.72 mm. Rainflow algorithm was used to the estimate temperature means and temperature variations. Palmgren–Miner rule [140] was used to calculate accumulated damage and to estimate reliability. This rule was also considered by Kostandyan and Sørensen [141] for deriving a reliability estimation method for an IGBT power electronic module. Based on the proposed model, a life prediction with crack movement was also described. Wang et al. [142] presented a reliability enhancement by integrating (liquid cooling structure in IGBT module. More than 50% junction to heat sink thermal resistance deduction was archived by direct liquid cooling.

Condition monitoring is one effective method for enhancing reliability and improving device life time. Degradation process of a 400 A IGBT power module was monitored in a real time system by Watanabe et al. [143] under power cycling test. Acoustic tomography was used to

monitor the device chip temperature and reliability model was derived based on the obtained temperature profile.

In the review study presented by Yang et al. [144] which investigates condition monitoring methods for power electronics, dominant failure mechanisms were described. The benefits and limitations of these techniques are discussed as follows; the understanding of the failure mechanisms and effects should be enhanced. Also, system terminal characteristics degradation without using sensors but within embedded in the module might be a realistic and promising approach regarding to sensitivity. A combined condition monitoring and measurement technique would be ideal with reliability modelling to estimate lifetime prediction and prognosis for systems in service.

Another review study stated by Song and Wang [145] discuses that power electronic manufacturing perspective is effective at the beginning phase of system design and active thermal managements is effective on the existing hardware in terms of reliability enhancement. Active thermal management systems are designed to regulate steady state and transient thermal-mechanical stress in power electronic modules of operation. System parameters can be controlled such as switching frequency and load current regulations according to the maximum junction temperature to guarantee junction temperatures of all devices below a critical value.

2.4.1 Reliability of ElectroThermal Performance of Silicon and Silicon Carbide Technologies

Increased lifetime demands for PECs especially in renewable energy applications have necessitated deeper investigation into the reliability of such systems. Latest manufacturing technologies of IGBTs have led to thinner silicon- and trench-gated devices [146]. Negative temperature coefficient of collector-emitter voltage, $V_{CE(sat,)}$ in punch-through (PT) created a high risk of thermal runaway when paralleling the devices. Another planar gate generation without *n+* buffer layer was the Non-Punch-Through (NPT). Inspite of the positive temperature coefficient of $V_{CE(sat),}$ conduction losses increased due to longer channel which causes poor thermal properties.

To overcome the downsides of the planar gate devices, vertical, trench gate technology has been developed [147]. Charge injection enhancement, reduced tail current at turn off and decreased power loss profiles were achieved by this technology [148],[149]. Since the

voltage drop over the channel is inversely proportional to the channel width and proportional to the length of the channel, lower conduction losses were achieved by shortening the channel [150]. For instance, trench gate devices can provide around 30% power dissipation deduction for 600 V IGBTs, typically optimized at 20 kHz switching frequency, in DC-to-AC inverter applications [151] [152].

Further improvements were achieved by a field stop (FS) region which is added to thin-wafer NPT device. This layer stops the electric field and allows high breakdown voltage through thinner wafer[153]. It results in faster switching capabilities, higher current density, as well as lower saturation collector to emitter voltage and 40% reduction in the conduction losses. Electro thermal physics-based model for the FS was developed by Kang et al [154]. Practical studies were proposed by Forsyth et al. [155] to parameterise a physical IGBT model, for three generations of IGBT, using double-pulse switching test, at temperatures extending down to 50°K.. Effects of different parasitic circuit characteristics of NPT and FS topologies have also been presented by Bakran et al.[156]. More IGBT cells are used with thinner silicon for even lower on-state voltage and improved switching characteristics. Higher switching speed is leading to lower switching losses but causes EMI whilst keeping the turn on losses low due to gradual change in voltage with respect to current [157]. Thermal profile improvement and monitoring is one essential reason of technological improvements. Comparison of junction temperature evaluations in IGBT modules in [158] [159] as well as the measurement and modelling of power electronic devices at cryogenic temperatures have been studied in [167] . Characterization of high-voltage IGBT module degradations under PWM power cycling test at high ambient temperature has also been assessed in [161].

A number of FS topologies have been produced by different manufacturers to maximise efficiency by optimizing carrier concentration; to minimize overall losses and operating temperatures by increased channel width and cell density. For instance, high resistivity substrate and finite drift layer thickness requirements were solved by super-junction field stop (SJFS) IGBTs [162] with charge balance concept. Soft-Punch Through (SPT) IGBTs [163] with positive temperature coefficient were developed based on same concept. Integration of freewheeling diodes, within IGBTs can also be counted as major improvement by use of

shorted-anode (SA) technology for reverse current conduction feature [164]. In FS IGBTs, FS layer provides enough breakdown voltage at backside structure. Hence, it has higher switching speed capacity and lower switching losses. In literature, Chibante et al. studied physics based models for NPT [165] and PT IGBTs [166] for hole/electron distribution based on ambipolar diffusion equation . Takaishi et al. [167] studied analytical formulation turn-off waveform for advanced trench gate IGBTs under high current density condition for calculating trade-off curve between turn-off loss and saturation voltage. Ronsisvalle et al. [168] proposed an experimental characterization for the input capacitance of FS Trench IGBTs. In contrast, accurate electro thermal modelling and temperature monitoring of IGBT's depend on collector tail current and collector to emitter saturation voltage. Thus, power sensing elements have to be coupled within electro thermal model accurately. Tang et al. [169] proposed FS switching transient model for simulating the turn-off tail current switching transient of IGBT at different temperatures. It was analyzed that base excess carrier lifetime has a great influence on the temperature characteristics of switching transient and thermal behavior greatly changes during on and off times. Dynamic avalanche on PT IGBTs to locate active areas of chip region and thermal analysis using FE simulations were studied by Lefranc et al. [170]. Yet, parasitic elements of IGBTs such as carrier mobility, excitation concentration and trans conductance vary with temperature [169]. Hence the performance of IGBTs in terms of on-state voltage, tail current, switching speed and lifetime are affected [171]. Many studies present FE models of power modules for thermal impedance characterization and derive thermal models based on the generic current signals. In fact, limited amount of data is supplied by the manufacturer datasheets for the switching characteristic although the listed properties above are temperature depended. This can cause vital changes in the electro thermal performance of IGBTS based on the application type they are used with [172]. A reliability study presented by Khosroshahi et al. [173] showed that IGBT technology was used and operating modes of the converter matter on overall life time.

Recent studies are taking places for fabrication of high performance SiC MOSFET which reduces power losses especially at high carrier frequencies [174]. Analytical formulation of injection capability of SiC device has been proposed by Lee and Huang [175]. Degradation characteristics and features of SiC devices have been presented in [176] [177].

Takao and Ohashi [178] proposed a novel power loss estimation method based on an analytical model of Si-IGBT and SiC diode pairs to investigate suitability of coupling of two technologies. Power losses of the tested devices were calculated to investigate the upper limitation of the switching frequency and the method was validated by comparing the calculated and measurement results. By using the proposed method, the high voltage 4.5-kV Si-IGBT was found appropriate at 2.9-kHz to be used with the SiC diode.

Zhong et al. [179] presented a prototype development of an 800 kHz, 800 V output boost dc–dc converter module which integrates SiC MOSFET and SiC Schottky diode die. An FE model of the converter was also studied by using ANSYS simulation. The experimental and simulated junction temperatures were found approximately equal to each other (≈320 ℃) when the total SiC MOSFET chip loss was 147 W. It was observed that the solder layer temperature was 198℃, which indicates that the solder layer was completely molten. This proved that the reason for the thermal resistance increment is gradual after the junction temperature exceeds 180℃. As a result, it was proposed that high frequency gate driver capability at temperatures greater than 300℃ for needs to be obtained to enable SiC power devices operating beyond 320◦C junction temperature. Regardless promising material properties of SiC, Si devices can still be more reliable and economically efficient based on the current rating and switching frequency of a specific application.

2.4.2 Lifetime Performance and Thermal Reliability of PECs in Wind Energy Applications

Wind energy has become one of the fastest developing renewable energy technologies. The performance and lifetime of these systems highly depend on PECs. They suffer from reliability related issues caused by variable and unpredictable wind and other natural effects [180]. Due to their ease of driving and higher frequency switching capacities compared to other semiconductor devices, insulated gate bipolar transistors (IGBTs) found their wide applications in PECs. Malfunctions of PECs cause failures to electrical/control systems within wind energy systems and contribute to approximately 41% of the total causes [181]. In literature, Senturk et al. [182] studied a thermal power capability determination algorithm for different multilevel topologies consist of press-pack IGBTs of grid side wind system converter. Blaabjerg et al. [183] presented another case study for providing life time prediction and temperature cycling analysis of PECs wind energy systems. DC link voltage

adaption is also one of the promising choices for PECs in terms of reliability and life time extension [184]. In renewables either in solar, [185] or wind [186] systems, controlling the DC bus voltage is already important for maximum power point tracking (MPPT), avoiding distorted energy generation and grid interfacing. El-Sousy et al. [187] studied a DC link voltage regulation model for a grid connected FS wind system in order to provide an MPPT technique. Bekakra and Attous [188] also developed a DC link voltage control method for a back-to back converter connected to a variable speed wind turbine. In these control strategies, the main aim is to keep DC voltage steady. However, it is also possible to operate these systems with dynamic DC link voltage as discussed by Dayarante et al. [189]. Lower DC link voltage can decrease the power losses [190], [191]. However, it would also cause large fluctuation and hence larger thermal in the grid side converters. Especially, this should be avoided at low switching frequencies for protecting the utility grid inverter from highly distorted AC signals. Monitoring the DC link current and voltage ripple analysis proposed by Pei et al. [192] or constrained optimal current control adoption method studied by Lemmens et al.[193],[194] can be two options for protecting the generator side converter from such worse case scenarios. However, based on the grid power requirements, operating at constant switching frequency would cause higher switching losses due to the higher current injection to grid side if DC link voltage is not sufficient. Therefore, controlling the switching frequency becomes crucial for the dynamic DC link voltage adaption methods. Recently, Andresen and Liserre [195] analysed the thermal cycles of the junction temperature in dependence of current and switching frequency and they derived a switching utilization method for an electrical vehicle by using space vector modulation (SVM).

Honsberg and Radke [196] studied the effect of the influence of power factor variation on the thermal behaviour of the IGBT chips located on a three level inverter device used in power factor correction systems. It was stated that each chip is affected by the power factor individually. On the other hand, the origin of power loss is changing i.e. while power factor is 1, lower chip mainly heated by conduction loss and when the power factor is -1, total losses are due to the combination of conduction and switching losses.

Ma et al. [197] studied the reactive power influence on the thermal cycling of power devices in grid-connected inverter for 10 MW wind turbines. By controlling the reactive power

circulated among paralleled converters, they proposed a new method to stabilize the thermal fluctuation of the associated power electronic converters during wind gusts. To achieve that, reactive current during the lower wind speed of a wind gust was injected and the junction temperature fluctuation in the most stressed devices was stabilized.

Ma et al. [198] also extended their studies to increase the lifetime of IGBT and diode chips during wind speed variations. A control method was derived to relieve the thermal cycling of, by circulating reactive power among the parallel power electronic converters. The amount of reactive power is adjusted to limit the junction temperature fluctuation in the most stressed devices. It was discussed that the technique is needed to be further investigated for adopting the grid requirements.

2.4.3 Comparison of the MPPT Methods and Lifetime of the PECs in PV Energy Systems

PECs are widely used in solar PV applications. The efficiency of PV systems is highly influenced by the irradiance level and load variations. Therefore, PECs are embedded as DC/DC converters within solar energy applications to ensure extracting the maximum power under different operating condition. This is known as Maximum Power Point Tracking (MPPT) and is a control strategy which can be achieved via a number of methodological approaches. Two most popularly algorithms are present in research literature and industry; Perturb and Observe (P&O) [199] and Incremental Conductance (IC) [200] methods. Many studies have been proposed in order to improve the existing MPPT methodologies in literature in terms of efficiency, tracking speed and MPPT accuracy. Zhang et al.[201] proposed a MPPT method which uses a sliding mode control strategy by controlling the duty cycle of a buck converter and it achieved efficiency improvement of 5%. Moradi and Reisi [202] studied another algorithm, first by setting point calculation to approximate the MPP based on the open circuit voltage [203]; then by using a fine tuning loop based on P&O method. Quoc et al. [204] also proposed a similar combinational MPPT algorithm by employing the IC. Kabalaci et al. [205] improved the P&O algorithm with extended PI controller for a hybrid solar and wind energy system. Maranda and Piotrowicz [206] used recorded real-life irradiance data to study static and dynamic performance of P&O algorithm by using a narrower time resolution. Haroun et al. [207] developed a PV system consisting of

two cascaded boost converters and derived a design oriented averaged model including MPPT controller which can achieve 95% efficiency.

Comparison among MPPT algorithms was also widely studied. Liu et al. [208] compared the conventional P&O method with an improved version and 93% efficiency was achieved while this was 72% for the conventional one. Houssamo et al. [209] presented experimental comparison between P&O and IC algorithms for maximizing the output power from a PV. Same algorithms were also compared in terms of PV voltage ripple, dynamic response and experimental tracking factor (TF) by using PV systems in [210] attached to boost and in [211] to a buck converter. Suitability of employment of the other DC/DC converters such as Buck-Boost and Cúk converters in P&O and IC algorithms for MPPT purpose was also compared in [212], [213]**.** Azevedo et al. [214] studied the effects of the improvements on both algorithms such as adjustment of the sampling rate, perturbation size etc. Ishaque et al. [215] on the other hand stated that IC method is slightly better since it gives 98.5% MPPT efficiency compared to 98.3% of P&O, based on a study conducted with a buck–boost MPPT converter attached to a PV array simulator. It was also observed that the performance of IC is highly depended on its step size, especially at low insolation levels. Dash et al. [216] proposed that although the P&O algorithm is easier to implement, IC is more accurate under rapidly changing irradiance conditions. Other MPPT techniques were compared in [217] based on their control variables and used circuitry for a PV system. Digital signal processing (DSP) controller feature of dSPACE real time interface (RTI) system is widely used in literature for implementing MPPT algorithms and to provide duty cycle control signal for PECs employed within PV systems. For instance, Mahdi et al. [218] implemented an improved P&O algorithm to ensure optimal operating points of a PV system using dSPACE DSP controller. Noman et al. [219] [220] presented another MPPT facility by using intelligent fuzzy logic controller designed in Simulink and operated within a PV system by using dSPACE 1104 software. Mathematical equations which describe the nonlinear characteristics of a PV panel to design a MPPT can also be implemented by using dSPACE as presented in [221]. However, in the literature, to the best knowledge of the authors of this article, no comparative study has been presented about the electro thermal effects of the MPPT algorithms on the DC/DC converters employed within PV systems, although temperature influence and importance of the electro-thermal design were mentioned in [222] ,[223] and

an improved thermal profile for PV inverters was assessed by power limit control method within P&O method in [224]. Most of the studies focused on comparing the tracking efficiency, signal ripple, speed response, sensitivity to environmental conditions, ease of hardware and software implementation and converter suitability among MPPT methods. However, life time of the DC/DC Converter which operates the MPPT has vital effect on the reliability of the solar PV application which is embedded. Operating principles of each MPPT algorithm also differ from each other. This produces different power loss profiles which cause dissimilar operating temperature amplitude and fluctuations for PECs. Therefore, the operational difference characteristic is essential to be explored for reliability assessment among MPPT algorithms.

2.5 Summary and Research Question

From the above mentioned research work, it was noted that reliability of the power electronic devices is one of the most significant factor which affect the overall lifetime of the renewable energy systems. Many techniques have been proposed to accurately monitor the thermal profile of these devices and predict the remaining lifetime. New material types, cooling component improvements and lead-free soldering techniques are highlighted examples of possible reliability extension methods in literature. Thermal stress is also defined as the main cause of the fatigue occurring and eventual failures between the bonded layer materials. However, few publications appear in literature which concerns to decrease these stresses by optimising the power losses of power electronic converters. Therefore, this research work will focus on developing efficient control algorithms to minimize the thermal stress; hence to increase their life time. Also, new thermally high conductive material types such as SiC for IGBT chip manufacturing is further investigated in order to achieve less thermal stress profiles for semiconductor devices. To achieve this aim, the following objectives are executed;

- A three dimensional finite element model (FEM) is implemented for accurate estimation of thermal profile of a power module. Based on the thermal characteristic obtained by the FEM, an electro thermal model was developed to predict the temperatures of each layer of the power module that cannot be measured during service.

- Recent topological improvements have led design of new devices called Silicon Carbide (SiC) MOSFETs which are also being used as switching elements for PECs. However, no rigorous investigation has been carried out to assess the effects of design and construction techniques on thermal behaviour under different operating and environmental conditions in literature. A detailed investigation into the performance of those switching devices with a focus on their reliability and thermal characteristics was studied and compared to the three types of differently manufactured insulated gate bipolar transistors (IGBTs). Namely, punch through (PT), non-punch through (NPT) and field stop (FSTP) silicon trench gate technologies.

- Based on the surveyed research work, thermally induced effects, e.g. thermal stress caused by temperature fluctuations, of the dynamic DC link operation have not been thoroughly analysed in literature. This research offers a new switching frequency driving scheme, based on the optimised DC link voltage requirements to decrease thermal stress across power electronic modules.

- Most of the studies in literature focused on comparing the tracking efficiency, signal ripple, speed response, sensitivity to environmental conditions and ease of hardware and software implementation and converter suitability among MPPT methods of PV systems. However, life time of the DC/DC Converter which operates the MPPT has vital effect on the reliability of the solar PV application which is embedded. Operating principles of each MPPT algorithm also differ from each other. This produces different power loss profiles which cause dissimilar operating temperature amplitude and fluctuations for PECs. Therefore, the operational difference characteristic is essential to be explored for reliability assessment among MPPT

algorithms. This work investigates the effects of IC and P&O maximum power point tracking algorithms on thermal stresses and reliability of PEC modules.

- Adjusting the switching frequency is one of the modelling techniques for power loss and thermal stress reduction as discussed in literature. To expand these models based studies, an experimental validation and accurate FE modelling for a three phase inverter power module is implemented and examined under various operating conditions. The model is experimentally validated via dSPACE real time implementation of actual inverter and with a physical permanent magnet generator based wind turbine system test rig.

Chapter 3

Electro Thermal Modelling of Power Electronic Modules

3.1 Overview

Implementation of an electro thermal, 3D finite element model for a multichip single IGBT power module is presented in this chapter. The model was built with COMSOL finite element package. Based on the thermal profile extracted from Finite Element (FE) analysis, a compact electro thermal model was implemented in discrete z-domain with MATLAB/Simulink for continuous temperature estimations over each layer based on the heat interactions and coupling effect across IGBT/diode chips.

3.2 Physical and Electrical Properties of IGBT/Diode Power Electronic

Power semiconductor devices are the essential components of power electronic systems (PECs), used for renewable energy conditioning. The Insulated Gate Bipolar Transistor, IGBT, is one of these components that can be operated as a switching element for a power electronic conversion unit. The first IGBT was demonstrated by Baliga in 1979 [225]. After comprehensive improvements, it was commercially introduced in 1983 [225]. The symbol and the equivalent circuit of IGBT device are shown in the Figure 3.1 (a) & (b).

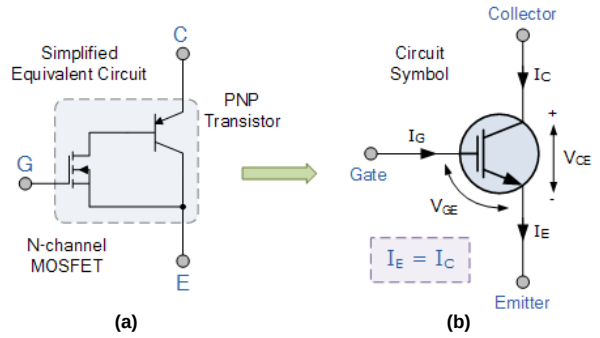


Figure 3.1 (a) Simplified Equivalent Circuit and (b) Circuit Symbol of IGBT [226]

The device combines easy driving advantages of MOSFET and the low on-state voltage of bipolar transistor technologies [227]. The basic construction is very similar to a MOSFET but with an extra P+ substrate layer, called collector and with an emitter terminal instead of source. The cross-sectional view of an IGBT device with locations of the equivalent devices can be represented as in Figure 3.2.

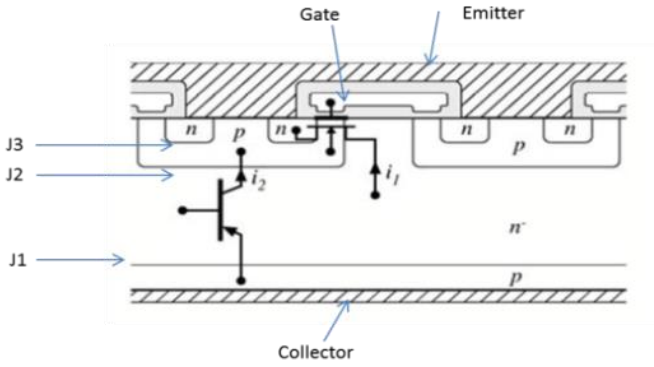


Figure 3.2 Cross-Sectional view of an IGBT

The physical working principle of the device is mainly divided into three sections [228]. First, when negative voltage is applied on collector to emitter, there are no current flows through the device for the lower junction, J1. This is called the reverse blocking mode. The forward blocking mode on the other hand is the operation when positive voltage is applied to the collector and the gate to emitter voltage (V_{ge}) is equal to zero. In this case, the upper junction, J2, is reverse biased. When a positive voltage higher than the threshold voltage is applied, the device is in the on state operation. This leads the p region to be inverted to an n channel then electron flow starts through n region of emitter to n drift region J1 and J2. The more positive voltage is applied, the more injected holes concentration is processed [228]. This operation is limited by the capacity of the n channel and stops when collector to emitter current reaches to the saturation point where active region begins. The characteristics of voltage (V_{CE}) vs current (I_C) through device explained above are shown in Figure 3.3, below.

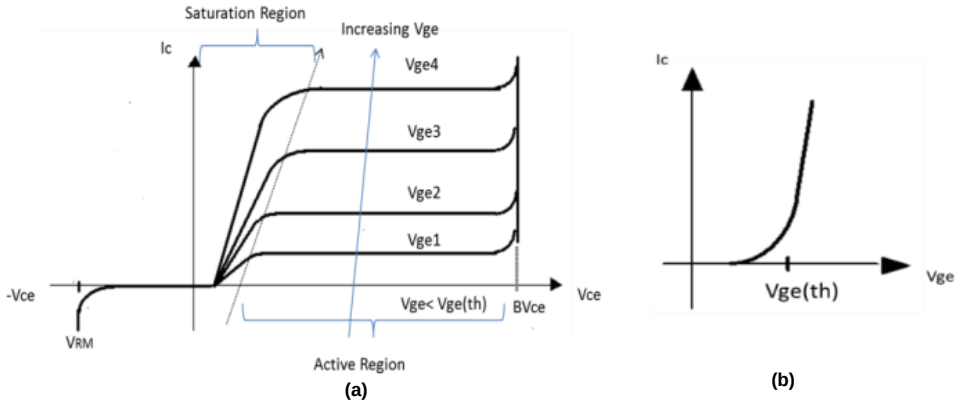


Figure 3.3 (a) Ic vs. Vce & (b) Ic vs. Vge characteristics of IGBT

Dynex Power Electronic Module, DIM1200ASM45, shown in Figure 3.4 (a); was studied and modelled in this chapter which is applicable for wind energy applications. Circuit

configuration of the device is shown in Figure 3.4 (b). It is manufactured as a single switch IGBT/Diode module with 24 IGBT and 12 diode chips. It has maximum collector current of 1200 A and collector-emitter voltage of 4.5 kV [229]. This device was particularly chosen since it is suitable for both single and three phase applications and can be tested in laboratory environment as a switching element by itself only.

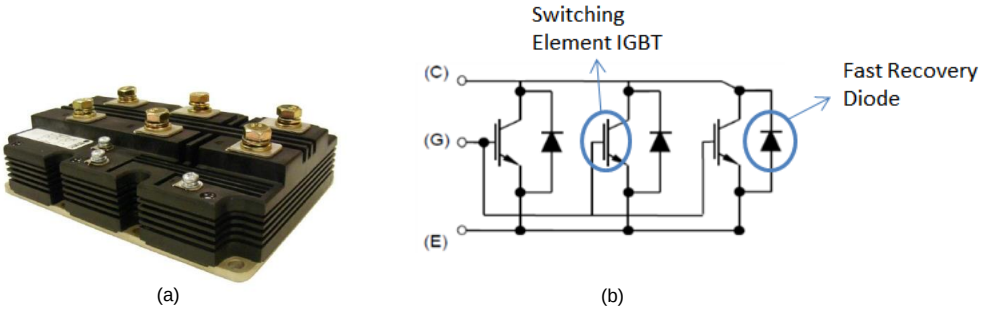


Figure 3.4 (a) Physical view (b) Circuit configuration of power module DIM1200ASM45

The built purpose of the antiparallel freewheeling diodes is similar to conventional diode scheme as it provides a path for reverse current to bypass the IGBTs. This connection brings the advantages of bidirectional switching ability to avoid damages caused by reverse currents [230]. Figure 3.5 represents a scheme of the internal view of the power module.

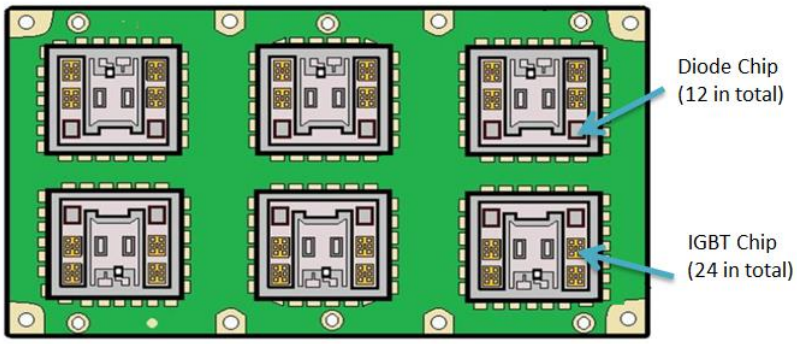


Figure 3.5 Internal view of DIM1200ASM45

Current and voltage characteristics of IGBTs and diodes in DIM1200ASM45 are as shown in Figures 3.6 a & b at 25°C and 125°C [229]. All chips in the module are in parallel. Hence, IGBT chips temperature increases at the same time when the device is on; and same for the each diode chip at off condition by sharing the total current through the internal resistance of the device. Thus, mean current flowing in each individual chip, $i_{chip,}$ can be represented as [104];

$$i_{chip}(t) = \frac{|i_{load}(t)|}{N} \tag{3.1}$$

where i_{load} is the total device load current and N is the number of chips. Based on the eqn. 1.1 current vs. voltage characteristics for each chip can be depicted as shown in Figure 3.6 (c) & (d). It can be observed that as temperature inclines from 25 °C to 125 °C, voltage drop across the module increases when the current level passing through the device is identical.

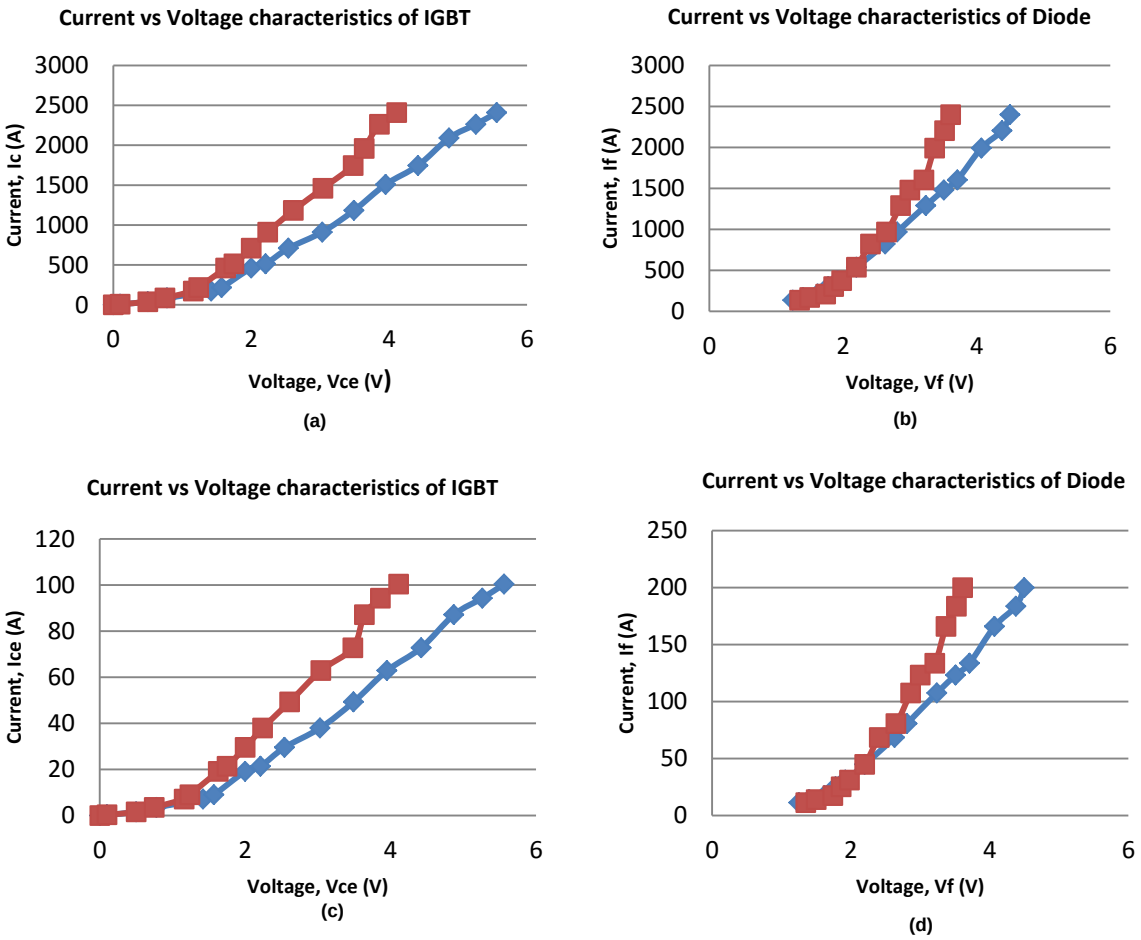


Figure 3.6 Current and voltage characteristics of a) IGBTs, (b) Diodes and (c) & (d) for each individual chip (T=125 °C, T=25 °C) [229]

Current and voltage characteristics of the device presented in Figure 3.6 are used to define the conduction power losses in the following section. In order to calculate the overall losses as a function of temperature, look up tables (LUTs) are used in Simulink.

3.3 Energy and Power Loss Modelling

Developing a proper electro thermal model strictly requires accurate power loss calculation and integration of the heat generation represented by internal self-heating and cross coupling effects across each chip and layers underneath. During recovery, heat generation also occurs among neighbour and adjacent layers due to the reverse current over diode

chips which also affect the mean temperature. Power losses with respect to the current and voltage signals are described schematically in Figure 3.7.

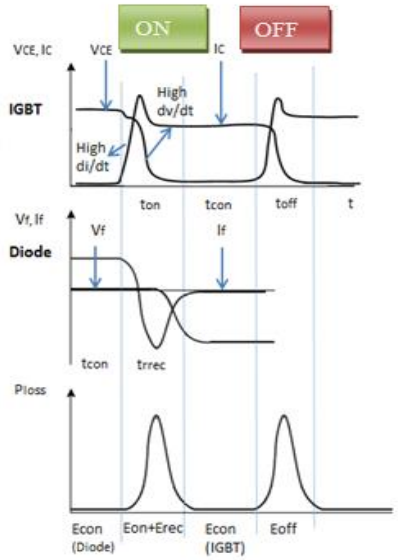


Figure 3.7 Characteristics of IGBT and Diode energy losses with respect to voltage/current and switching behaviour

During switching process, the stepper change in *di*/*dt* and *dv*/*dt* causes the total switching losses which lead to increase in the temperature through the device. Switching energy losses for a single power electronics module, over one period of switching processes, is divided into Turn-on and Turn-off losses, $E_{SW,ON}$ and $E_{SW,OFF}$, for the IGBT. The instantaneous switching power losses, $P_{SW,IGBT}$ of IGBT can be calculated as[104],[14]:

$$P_{SW,IGBT}(t) = f_S \cdot \left(E_{SW,ON}(I_C(t)) + E_{SW,OFF}(I_C(t))\right) \tag{3.2}$$

where I_c is the IGBT collector current and f_s is the switching frequency. The average switching power loss of IGBTs, $P_{SW,IGBTAV}$ can be expressed as the integral of instantaneous power losses as:

$$P_{SW,IGBTAV} = f_o f_S \int_0^{1/f_o} \left(E_{SW,ON}(I_C(t)) + E_{SW,OFF}(I_C(t))\right) dt \tag{3.3}$$

where f_o is the fundamental frequency. Similarly, diode instantaneous recovery power losses, $P_{SW,DIODE}$, can be denoted by means of recovery energy, $E_{SW,RR}$, as:

$$P_{SW,DIODE}(t) = f_S \cdot E_{SW,RR}(I_F(t)) \tag{3.4}$$

where I_F is forward current across diodes. Average recovery power loss can be derived as:

$$P_{SW,DIODEAV} = f_o f_S \int_0^{1/f_o} \left(E_{SW,RR}(I_F(t))\right)dt \tag{3.5}$$

Average switching power losses, $P_{SW,AV}$, over IGBT and diodes within total number of cycle, N, in each fundamental frequency at n^{th} switching period can be denoted as [104], [16]:

$$P_{SW,AV} = f_o \sum_{n=1}^{N}\left[E_{SW,ON}(I_C(n)) + E_{SW,OFF}(I_C(n)) + E_{SW,RR}(I_F(n))\right] \tag{3.6}$$

Total conduction loss of power module is composed of the total IGBT/diode chips conduction losses, $P_{CON,IGBT}$ and $P_{CON,DIODE}$, respectively. The instantaneous conduction loss, P_{CON} can be derived as:

$$P_{CON}(t) = P_{CON,IGBT}(t) + P_{CON,DIODE}(t) = V_{CE}(I_C(t)).I_C(t).D_I(t) + V_F(I_F(t)).I_F(t).D_D(t) \tag{3.7}$$

where, V_{CE} is the collector-emitter saturation voltage of the IGBT. V_f and I_f are the forward conduction voltage and current of the diode, respectively. D_I is the conduction time of the IGBTs and D_D for the diodes. Average conduction power loss, $P_{CON,AV}$ can be expressed as the integral of instantaneous power losses as [2–28]:

$$P_{CON,AV} = f_o \int_0^{1/f_o} P_{CON}(t)dt = f_o \int_0^{1/f_o} \left[V_{CE}(I_C(t)).I_C(t).D_I(t) + V_F(I_F(t)).I_F(t).D_D(t)\right]dt \tag{3.8}$$

Average switching power losses, $P_{CON,AV}$, over IGBT and diodes within total number of cycle, can be derived as:

$$P_{CON,AV} = f_o \sum_{n=1}^{N}\left[V_{CE}(I_C(n)).I_C(n).D_I(n) + V_F(I_F(n)).I_F(n).D_D(n)\right] \tag{3.9}$$

Similar to the current characteristic of the device, energy loss distribution over each IGBT chip is approximately $1/24^{th}$ of all IGBTs and $1/12^{th}$ of the module diode losses for diode chips as [104] and [103] discussed. Hence, switching and conduction losses of power module and scaled down losses for individual chips can be represented as shown in Figures 3.8 & 3.9, respectively.

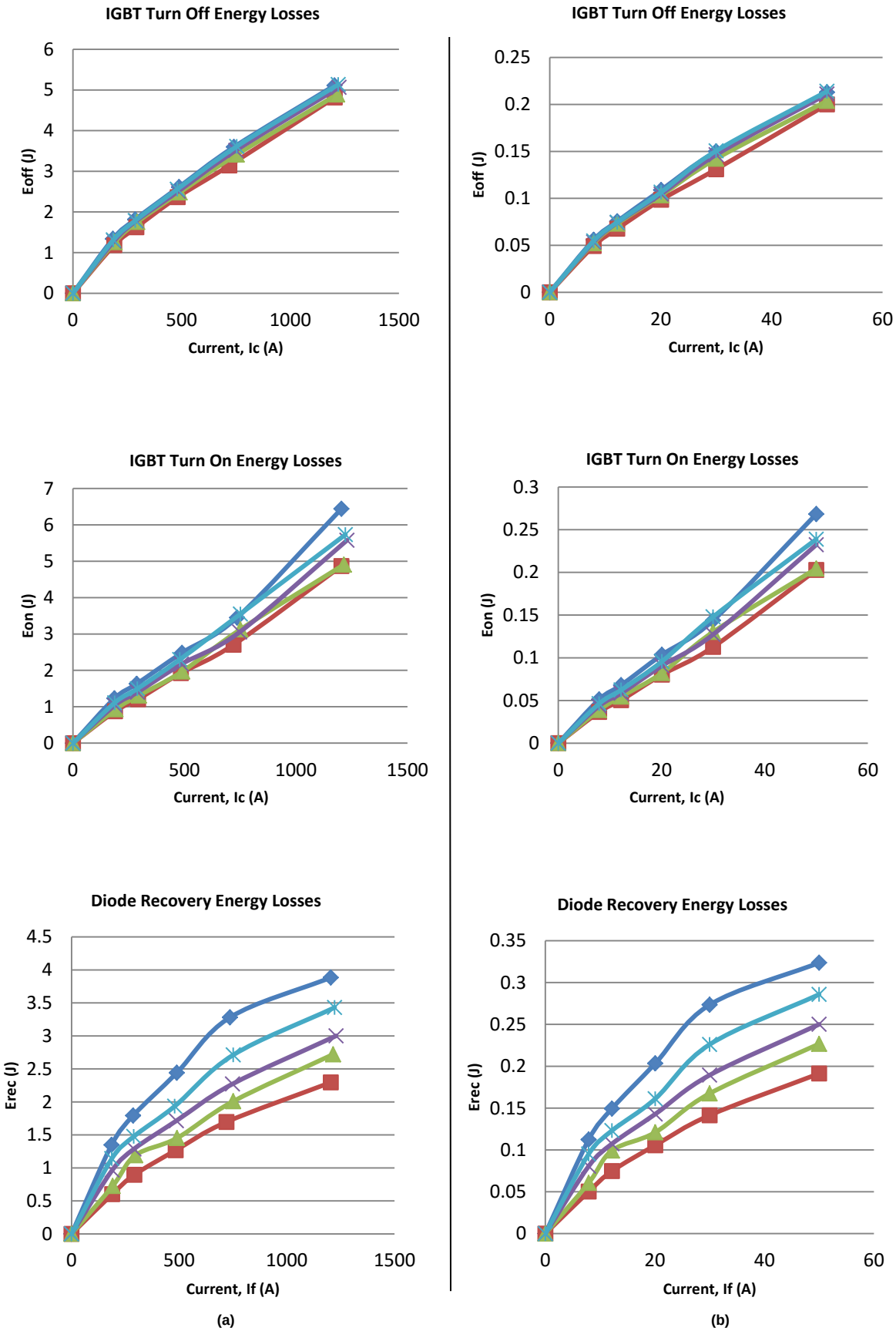


Figure 3.8 IGBT & Diode switching energy losses for (a) module (left), (b) for individual chips (right)

As it can be shown in Figure 3.8 b, the losses for IGBT chips are 1/24th of overall module losses (Figure 3.8 a) where these are 1/12th for diode chips. Also, as the temperature increases, the amount of the losses inclines. Different than the most of the power loss models in literature [91]–[94], individual chip losses data were used to implement the switching losses in LUTs. Those previous studies could not provide an accurate representation of losses of the power modules since parallel die chips have individual power loss profiles. This is because of the temperature depended power loss occurring is different for each chip, based on their geometrical position on the power module (coupling effect).

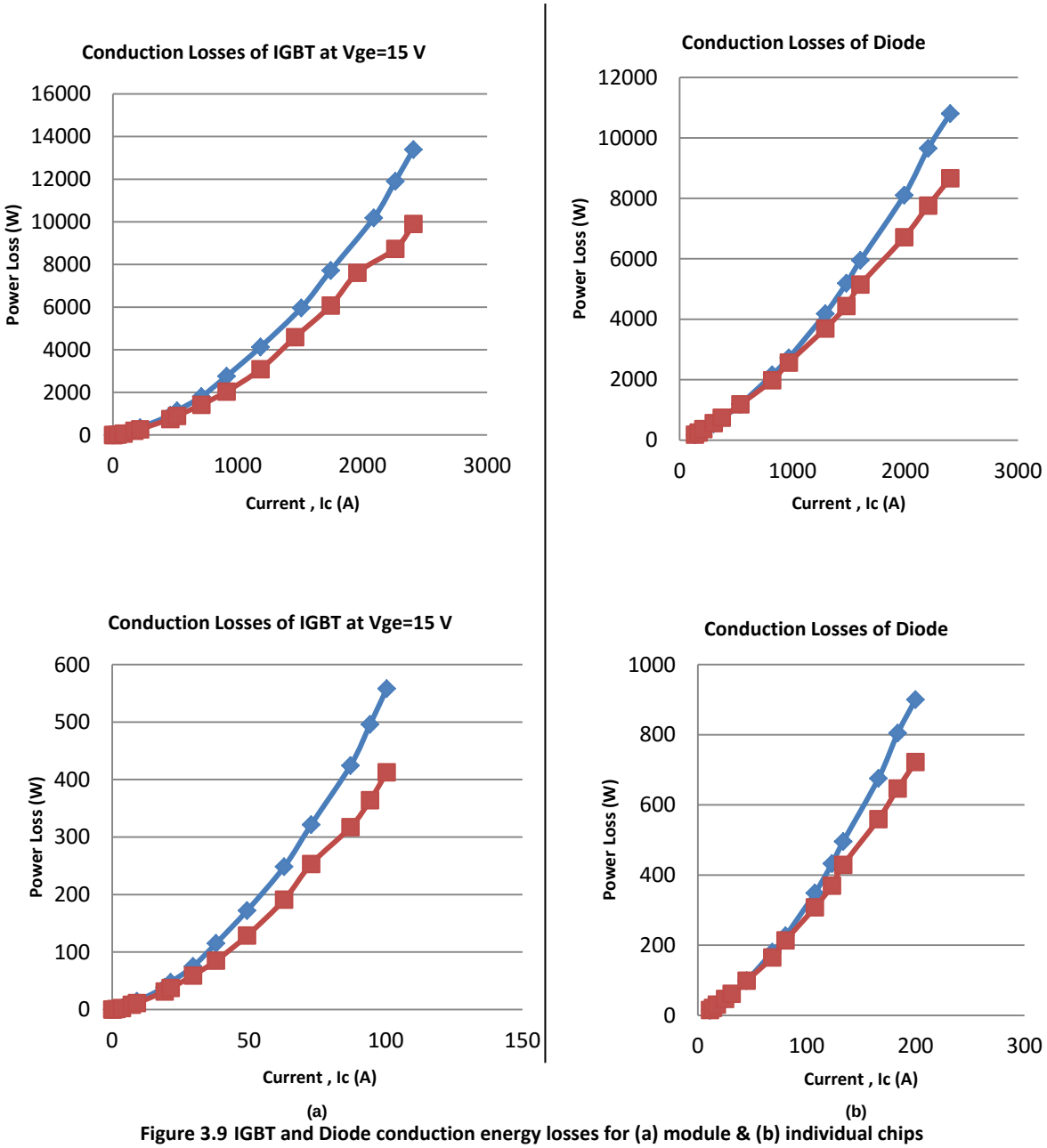


Figure 3.9 IGBT and Diode conduction energy losses for (a) module & (b) individual chips

(T=125 °C, T=25 °C) [229]

Overall and individual chip conduction losses are shown in Figure 3.9. As it can be depicted, since the current level is decreased 1/24th for each IGBT and 1/12th for each diode chip, the power losses are also declines by the same ratio. Power loss model is shown in Figure 10.

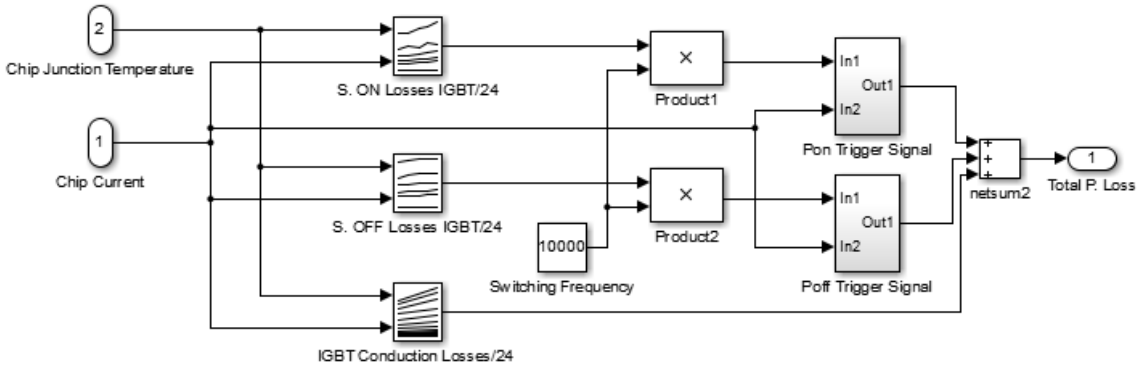


Figure 3.10 Sample Power Loss model for a single IGBT chip

In the power loss model, instantaneous switching and conduction losses are computed by LUTs based on the current/voltage characteristics of each chip defined in Figure 3.6 with respect to the instantaneous temperature. For instance, switching OFF losses data for IGBT chips (Figure 3.8 b) which was built in LUTs can be as seen in Figure 3.11.

Current (A)

Energy Losses (J)

Temperature(°C) \	0	7.91	12.16	20.08	30	50
25	0	0.0493	0.0676	0.0985	0.131	0.2
50	0	0.052333333	0.073041667	0.10325	0.142166667	0.203666667
80	0	0.053458333	0.074125	0.104583333	0.146458333	0.211041667
100	0	0.054666667	0.0745	0.106541667	0.1505	0.213916667
125	0	0.055791667	0.075583333	0.108916667	0.149958333	0.212916667

Figure 3.11 Scaled switch OFF losses for one single chip in Look up Table

Total power loss for each active device is calculated in each switching cycle. Switching power loss calculation is triggered by the edge detector before and after the switching condition durations for IGBT and diode chips. In order to produce actual power loss behaviour (seen in Figure 3.7), switching ON and OFF losses are triggered in turn on and turn off [229] times only. These losses are added to the conduction losses to find the total power losses. The instantaneous total losses are then averaged by using a weighted moving average block in order to avoid the undesired temperature ripples caused by small ON and OFF time transients [97]. The operation is controlled by sub models that were built with control blocks available in Simulink.

3.4 Thermal Modelling Methodology for IGBT/Diode Module

Heat or thermal energy is created by the motions of molecules and atoms [231]. Increase in motion of the atoms and molecules lead more heat or thermal energy created by any material. There are three different heat transfer mechanisms where the heat is transferred from one place to another; Conduction, Convection and Radiation [232]. Conduction is energy transport due to molecular motion and interaction [232]. In other words, it is the transfer of heat between substances that are in direct contact with each other. It is proportional to the temperature gradients in a system and is formulated by Fourier's law as:

$$q = -k\frac{\partial T}{\partial x} \tag{3.10}$$

where q is the heat energy flow density, k is the thermal conductivity, $\frac{\partial \mathrm{T}}{\partial x}$ is the temperature gradient. The materials that have higher conductivity can transfer the heat rapidly. Convection is the energy transport when groups of the molecules move from one hot to another cold medium by fluid flow. It generally happens between solid and fluid boundaries. It is determined by Newton that the ratio between total heat transfer and surface area is proportional to the temperature difference between a solid and fluid material. It is defined as:

$$q = h(T_s - T_f) \tag{3.11}$$

where h is the heat transfer coefficient, T_s and T_f are the temperatures of solid and fluid materials, respectively. Radiation is the heat transferred through wave energy. The waves are called electromagnetic waves since the energy travels in electric and magnetic waves. The net heat radiation rate is proportional to the fourth power of the absolute material temperature and can be expressed as:

$$q = \sigma\varepsilon A(T_h^4 - T_{hc}^4) \tag{3.12}$$

where T_h and T_c are the hot and cold plates, A is the area of the object, ε is the emissivity of the material and the σ is the Stefan-Boltzman constant. The thermal characteristics of each layer affected by heat flux must be determined precisely for an accurate thermal design of any semiconductor power electronic device. The heat diffusion equation can be used to describe the distribution of heat flux through any material as a function of position and

material properties. It can be used to give a solution for temperature variations of a defined region in the time domain caused by conduction heat transfer as;

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{q}{k} = \frac{\rho.c.}{k}\frac{\partial \mathrm{T}}{\partial t} \tag{3.13}$$

where *T* is the temperature, *k* is the thermal conductivity, *c* is specific heat capacity, ρ is the mass density and *q* is the rate of generation of energy per unit volume [231]. A simplified form of eqn. 3.13 can be derived as in eqn. 3.14 by using Laplace transform to solve the heat distribution within the power module as:

$$D\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) = sT - T_0 \tag{3.14}$$

where *D* denotes the diffusion coefficient, $k/\rho c$, *T* is the Laplace transform of the temperature and T_0 is the initial temperature. The thermal resistance R_{th} and capacitance C_{th}, are functions of the material properties, are derived from eqn. 3.13 as;

$$R_{th} = \frac{l}{kA} \tag{3.15}$$

$$C_{th} = c.\rho.A.l \tag{3.16}$$

where *l* is the length and *A* is the cross-sectional area of a heated path. (Please refer to Appendix for electrical and thermal description of resistance and capacitance by means of one dimensional heat diffusion equation for thermal and transmission line equation for electrical circuits).

3.5 Definition of Thermal Heat Path

Thermal impedance represents the description of the system behaviour in terms of temperature. In order to estimate this identity, a constant heat source is applied to a material and heated until the steady state temperature is reached. Then, the ratio of the difference between the initial (T_s) and final temperature (T_f) to the applied total heat power (P_o) gives the thermal impedance. The thermal impedance can be represented as:

$$R_{th} = \frac{T_f - T_s}{P_0} \tag{3.17}$$

It leads to estimate junction temperature, T_j, of a semiconductor device when any variable input heat source (i.e PWM, Sinusoidal) is applied. It can also be measured practically in the cooling operation when an externally applied power is switched off and the device is left to cool down until reaching to the ambient temperature. Heating and cooling phases can be seen in Figure 3.12.

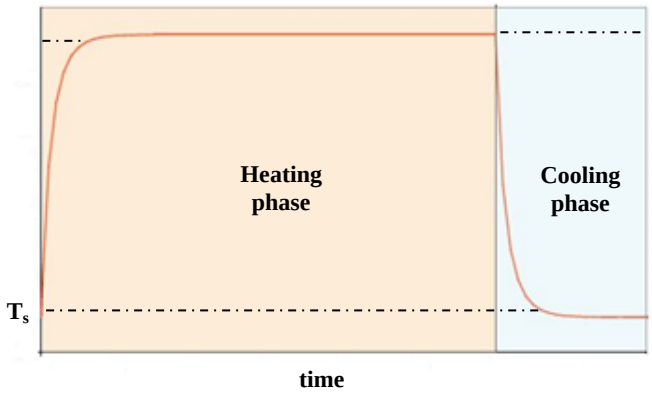


Figure 3.12 Heating and cooling operation of a solid material

Internal structure of typical power module and identified thermal impedance parameters are shown in Figure 3.13. Each device on the module consists of several layers. Each of them has different material properties; hence has different coefficient of thermal expansion. When heat is generated among these layers, deformation occurs due to the different expansion generation between these bonded layers, where eventual cracks occurs.

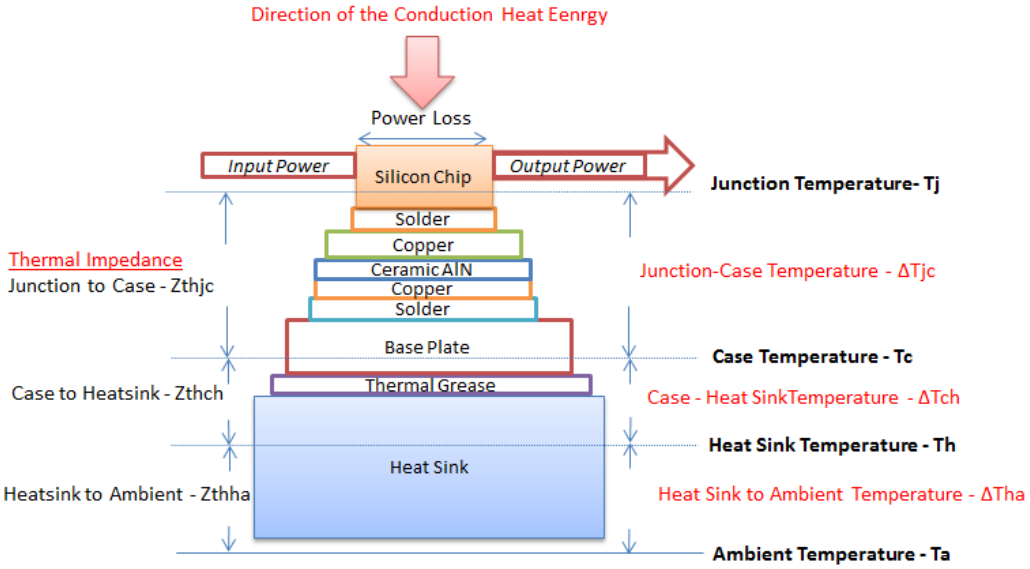


Figure 3.13 Internal Structure of a semiconductor device with thermal Impedances and temperatures identities

The junction temperature, $T_{j,}$ and the heat sink temperature, T_h, can be represented as shown in eqns. 3.18 and 3.19, respectively. In practice, the operating junction temperature has to be between the maximum and minimum allowed rating specified in datasheets, even in the overload conditions.

$$T_j = \quad T_h + Ploss\ (\ Z_{thjc} + Z_{thch}) \tag{3.18}$$

$$T_h = \quad T_a + (Ploss\ x\ Z_{thha)} \tag{3.19}$$

where T_a is the ambient temperature.

3.6 Cauer and Foster Thermal Networks

To represent the transfer function for each individual material, two commonly known thermal equivalent circuits, Cauer [56] and Foster models [57], can be used. The Cauer network has the advantages of describing the temperature distribution between the actual physical layers (die, solder, substrate, etc.) as shown in Figure 3.14. Each RC element represents the thermal resistance and capacitance of each layer. Foster network, on the other hand has cascaded mathematical form with parallel connected thermal resistance and capacitances as shown in Figure 3.15. Each RC element does not represent actual thermal identity of any layer [233]. The equivalent response has physical meaning for the junction layer, only.

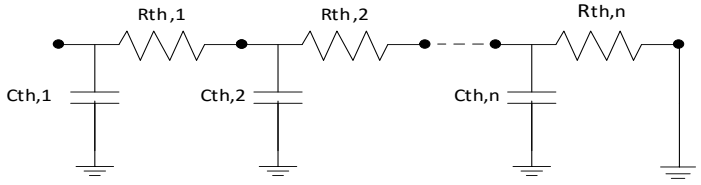


Figure 3.14 Equivalent thermal circuit of Cauer Network

The equivalent thermal impedance can be extracted for Cauer network as:

$$Z_{th}(s) = \cfrac{1}{sC_{th,1} + \cfrac{1}{R_{th,1} + \cfrac{1}{sC_{th,2} + \cfrac{1}{R_{th,2} + \cfrac{1}{\vdots \\ sC_{th,n} + \cfrac{1}{R_{th,n}}}}}}} \tag{3.20}$$

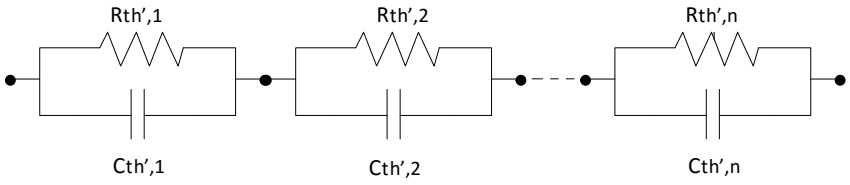


Figure 3.15 Equivalent thermal model Foster networks

Transient thermal impedance for each component with Foster can be represented as follows:

$$Z_{th}'(s) = R_{th}' \,//\, \frac{1}{sC_{th}'} = \frac{R_{th}'}{sR_{th}'C_{th}'+1} = \frac{\frac{1}{C_{th}'}}{s+\frac{1}{\tau}} \tag{3.21}$$

where;

$$\tau = R_{th}C_{th} \tag{3.22}$$

By taking the inverse Laplace transforms of eqn. 3.21, Z_{th} can be written in time domain as;

$$Z_{th}(t) = R_{th}(1-\exp(-\frac{t}{\tau})) \tag{3.23}$$

For *n* number of circuits, the total thermal impedance can be extended as:

$$Z_{th}'(s) = \frac{R_{th',1}}{sR_{th',1}C_{th',1}+1} + \frac{R_{th',2}}{sR_{th',2}C_{th',2}+1} + \cdots \frac{R_{th',n}}{sR_{th',n}C_{th',n}+1} \tag{3.24}$$

The data sheets provided by producers [229] contain thermal impedance information of the whole module based on the Foster network. Hence, conversion between Foster to Cauer network was studied by researchers [76], [78] in order to estimate actual layer dimensions to implement 3D FEM models. However, as stated by [234], this approach cannot produce the layer dimensions precisely since the thermal information supplied is only mathematical approximation form and does not have any physical meaning.

On the other hand, transformation of the thermal parameters from Cauer to Foster form is useful as it can contain each physical layer characteristics. Since the Foster for is a combination of parallel RC components, reduced order equivalences can be designed easier

compared to the Cauer form. As a part of this research, a new conversion algorithm from n^{th} order Cauer to Foster model is derived. (Please refer to Appendix for the derived algorithm of the transformation). An example, two layered (two RC components) Cauer to Foster conversion can be solved analytically as follows. The equivalent impedance for two layer Foster model is:

$$Z'_{thf}(s) = \frac{R_1'+R_2'+s(R_1'R_2'C_1'+R_1'R_2'C_2')}{1+s(R_1'C_1'+R_2'C_2')+R_2'+s^2(R_1'R_2'C_1'C_2')} \tag{3.25}$$

and equivalent impedance for two layered Cauer is:

$$Z_{thc}(s) = \frac{R_1+R_2+s(R_1R_2C_2)}{1+s(R_1C_1+R_2C_1+sR_2C_2)+s^2(R_1R_2C_1C_2)} \tag{3.26}$$

Given the actual physical layer dimensions and material properties, parameters R_1, R_2, C_1, C_2 of Cauer thermal network can be calculated from eqns. 3.15 and 3.16. Since it is desired to estimate equal response from the both configurations by equating numerators and denominators of eqns. 3.25 and 3.26 lead following solutions as;

$$R_1'R_2'C_1'+R_1'R_2'C_2' = R_1R_2C_2 = a \tag{3.27}$$

$$R_1'C_1'+R_2'C_2' = R_1C_1 + R_2C_1 + R_2C_2 = b \tag{3.28}$$

$$R_1'R_2'C_1'C_2' = R_1R_2C_1C_2 = c \tag{3.29}$$

$$R_1'+R_2' = R_1 + R_2 = d \tag{3.30}$$

By eliminating the eqns. 3.27 to 3.30, the solution eqn. 3.31 is derived as;

$$x^2(4c-b^2)+x(db^2-4cd)+(d^2c-abd+a^2)=0 \tag{3.31}$$

The solutions x_1 and x_2 are the thermal resistance parameters, R_2' and R_1' of the quadratic eqn. 3.13, respectively. By knowing the two unknowns R_2'&R_1', direct elimination between eqn. 3.29 and eqn. 3.30 should lead to find two unknown thermal capacitances, C_2' and C_1'. (Please see Appendix 2 for Analytical derivation of converted parameters for validation)

3.7 Heat Transfer and Thermal Modelling Implementation in Simulink

In order to verify the proposed Cauer to Foster transform, heat transfer through one single chip was initially modelled with electrical circuit blocks of Simulink. Based on the actual dimensions of the internal layers (i.e. Silicon die, Die solder, baseplate) and their physical properties, one directional, 8th order thermal model was generated for a single IGBT chip and the layers underneath as shown in Table 3.1.

Table 3.1: Physical Dimensions of layers of the DIM1200ASM45 Power Module

Layer	Physical Dimension			Physical Property		
	Length (mm)	*Height (mm)*	*Width (mm)*	*ρ(kg/m3)*	*k (W/mK)*	*c (J/kgK)*
Silicon, Die	13.55	0.375	13.55	2330	153	703
Solder	13.55	0.05	13.55	7360	33	200
Copper, Cu	16	0.3	45	8850	398	380
AIN	50.725	1	46	3300	180	750
Copper, Cu	58	0.3	49.3	8850	398	380
Solder	58	0.175	49.3	11300	35	129
Baseplate	190	5	140	3010	180	741
Grease	190	0.05	140	2800	1	705
Heat Sink	240	10	145	2730	155	893

Thermal capacitance and resistance parameters alongside the individual time constants were calculated for each layer by using eqns. 3.15 and 3.16 as seen in Table 3.2. Then, Cauer form of thermal model was derived from these parameters as depicted in Figure 3.16. Instead of a RC pair, a constant 25 V DC voltage source was attached to the Cauer model in order to represent 25°C heat sink temperature.

Table 3.2: Thermal Characteristics of each layer of the DIM1200ASM45 Module with Cauer

Layer	Thermal Characteristic (Cauer)		
	Cth(J/K)	*Rth(K/W)*	*τ (s)*
Silicon, Die	0.1127	0.01334	0.00150
Solder	0.0135	$8.2523.10^{-3}$	0.00011
Copper, Cu	0.726	$1.047.10^{-3}$	0.00076
AIN	5.775	$2.381.10^{-3}$	0.01375
Copper, Cu	2.884	$2.6361.10^{-4}$	0.00076
Solder	0.7294	$1.74.10^{-3}$	0.00126
Baseplate	296.644	$1.044.10^{-3}$	0.30969
Grease	2.625	$1.88.10^{-3}$	0.00493
Heat Sink	848.38	$1.38.10^{-3}$	1.17076

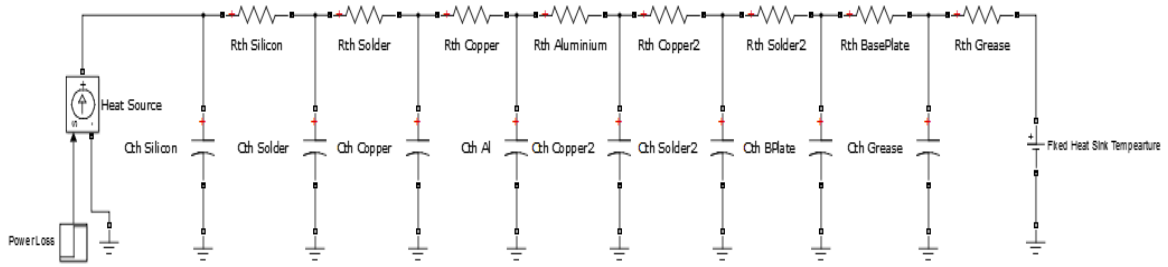


Figure 3.16 Equivalent thermal model of 8th order system using Cauer network

Then, the derived transformation algorithm was used to calculate Foster network parameters by MATLAB coding. The thermal identity for this circuit is shown in Table 3.3. Foster model implementation can be seen in Figure 3.17.

Table 3.3 Thermal Characteristics of layers of the DIM1200ASM45 Power Module for Foster Network Analysis

Layer	Thermal Identity (Foster)		
	Cth(J/K)	***Rth(K/W)***	***τ (s)***
Silicon, Die	6.347	$1.057.10^{-5}$	$6.71.10^{-5}$
Solder	$2.254.10^{8}$	$6.17.10^{-13}$	0.0001
Copper, Cu	5.508	$1.16.10^{-4}$	0.0006
AIN	$1.3548.10^{6}$	$1.28.10^{-9}$	0.0017
Copper, Cu	0.1263	0.02	0.0025
Solder	2.223	0.0015	0.0033
Baseplate	6.2421	0.005	0.0312
Grease	282.3906	0.0032	0.9036

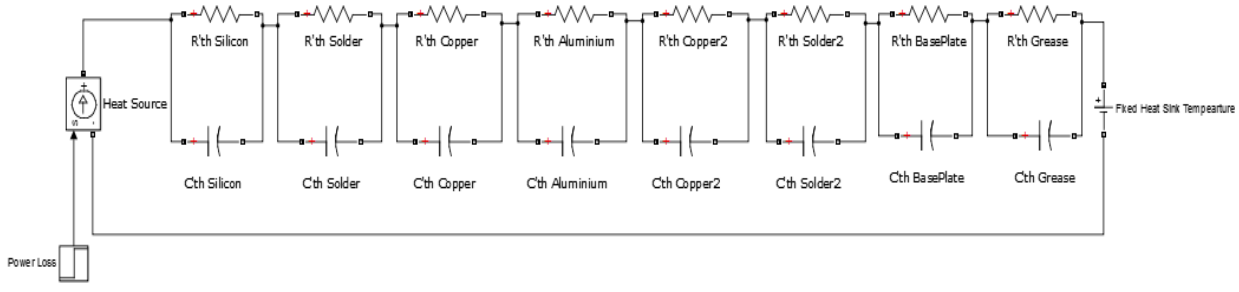


Figure 3.17: Equivalent thermal model Foster networks

The maximum conduction losses at 25°C was calculated as 133.2 W (for one IGBT chip ~ 50A) at full current (1200 A) from the data supplied by company. Hence, as an example, a

step input signal with amplitude of 133.2 was applied to the both circuits for representing an input heat source of 133.2 W. The results for both implementations are shown in Figure 3.18. It is noticed that the temperature at junction reaches approximately 29°C; hence simulation results showed good agreement and the conversion algorithm was verified.

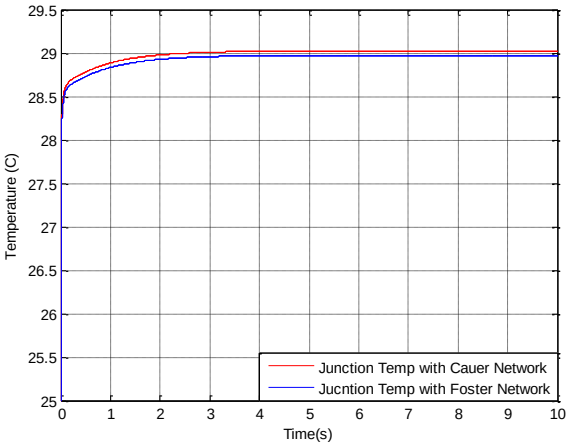


Figure 3.18: Comparison of Junction Temperature with Cauer and Foster Models

3.8 Validation of Preliminary Thermal Model with FEM

In order to verify temperature estimations obtained from the preliminary models, a 3D FE model of module which consists of only a single chip and layers underneath was implemented with COMSOL Multi-physics package. The material properties stated in Table 3.1 were used for constructing the geometry. Heat diffusion equation was defined for the whole model to solve the distribution of heat and temperature variations when an input heat power is applied. The ambient and heat sink temperatures were set to be 25°C and all outer boundaries are thermally isolated (no convection) to provide same test condition with circuit implementation discussed in previous section. Two dimensional power losses were applied to the upper surface of silicon chip as 133.2 W heat source as it can be seen in Figure 3.19.

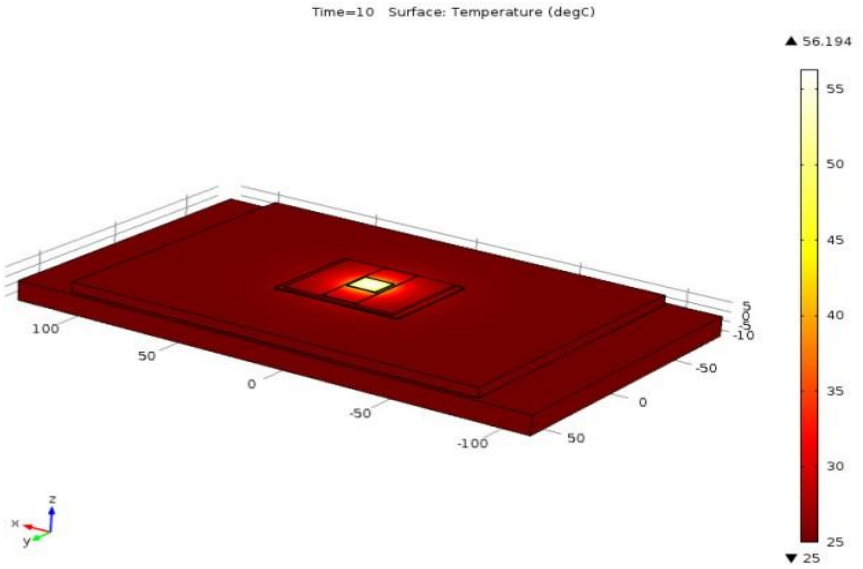


Figure 3.19: FE Model with of the one IGBT chip and layers underneath

The temperature estimations were observed from the geometric centres of each layer. Temperature at the each layer can be depicted from the Figure 3.20. The silicon die temperature at junction reaches to 55.1°C where this was only 29.04 °C in circuit implementation discussed in previous section.

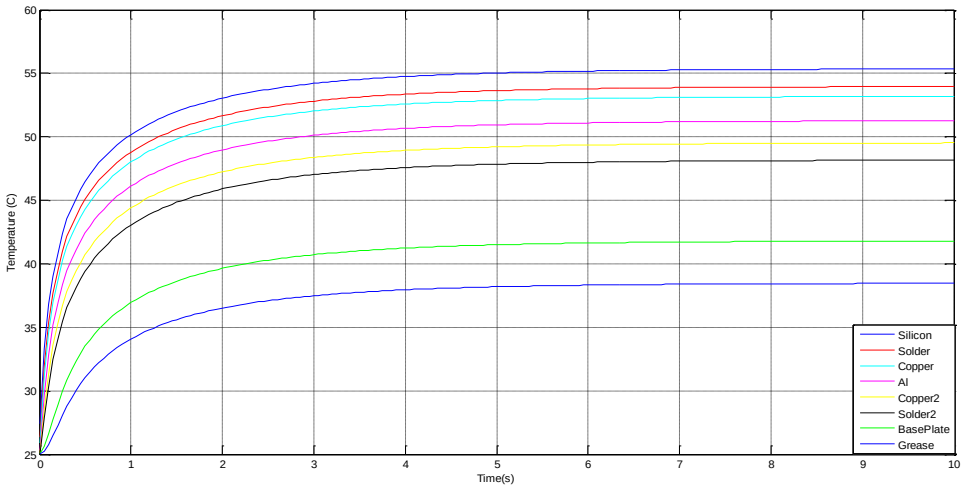


Figure 3.20: Estimated temperature distribution over each layer by FEM

Temperature contours over the layers and the total heat flux can be seen in Figure 3.21. The heat does not distribute homogeneously over each layer (due to spreading angle effect [72]). Heat flux direction was found as it follows a propagation angle along with z-axis as seen in Figure 3.22. The area affected by heat flux is observed as a circular region over the layers on the model. Therefore, defining the thermal resistance and capacitance parameters

(seen in Table 3.2) based on the actual geometric dimension (see Table 3.1) caused under estimations of temperatures in previous model since heat does not flow outer regions of circle.

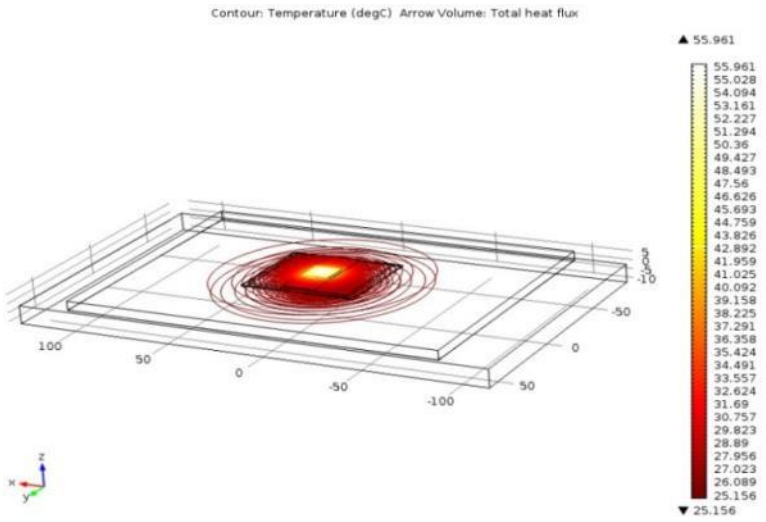


Figure 3.21 Heat flux distribution

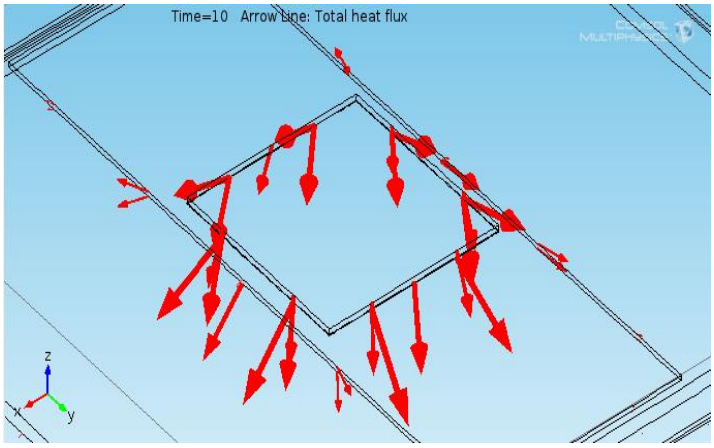


Figure 3.22 Heat Flux distribution directions

3.9 An Analytical Solution for Heat Path based on Spreading Effect

Self-heating effect on the layers was unable to be estimated correctly using actual dimensions of the layers caused by well-known spreading angle effect [72]. It occurs when a heat source area is smaller than the area of the following layer which consists of different material. Therefore, in this section, an analytical solution was studied for accurate heat and temperature observation. The heat diffusion equation considers hyperbolic problem which

leads circular heat propagation in its solution. However, for analytical simplicity, as also widely accepted in literature, [72], [81], it was assumed from FE analysis that heat follows a diagonal path with approximately 45° propagation. The heat source (chip) has a square shape; therefore in this work, it is accepted that the heat path follows a truncated square pyramid volume in z- direction as shown in Figure 3.23 a. The local cross sectional area of the heat flow path can be depicted in Figure 3.23 b and it was calculated as;

$$A = (a + 2.h.\tan 45)^2 \tag{3.32}$$

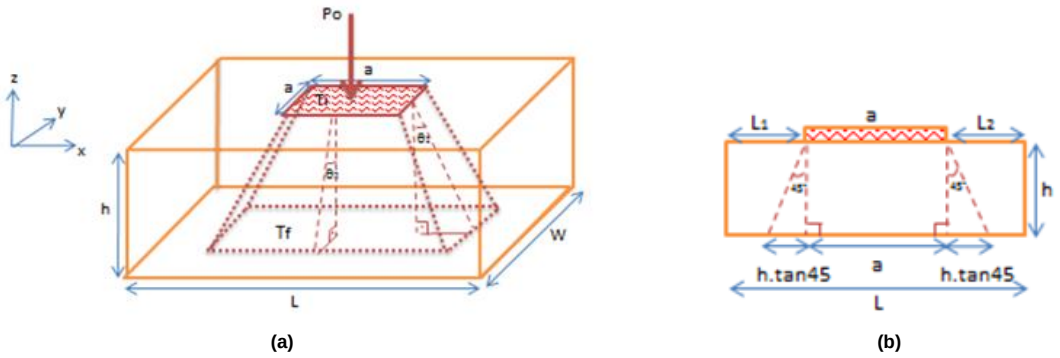


Figure 3.23: (a) Heat Flux distribution by constant spreading angle, (b) Lateral view of Heat Flux distribution

Area, *A* was replaced for calculating new thermal resistances of each layer in eqn. 3.15. Similarly, the total volume that is affected by heat flow can be written as;

$$V = \frac{1}{3}(a^2 + (2.h.\tan 45)^2 + (2.h.\tan 45.a))h \tag{3.33}$$

Volume, *V* was replaced with total volume element of thermal capacitance calculations in eqn. 3.16, as well. Then, by applying spreading angle analysis, new layer dimensions which are function of the approximated effective heat path are shown in Table 3.4 alongside the calculated thermal parameters *(Rth, Cth*). By implementing the Cauer Model with updated thermal parameters, analytical temperature distribution over each layer was estimated as seen in Figure 3.24 along with the FE modelling results.

Table 3.4 Physical Dimensions of approximated heat path for constant spreading angle

Layer	Physical Dimension			Thermal Identity (Cauer)		
	Length (mm)	*Height (mm)*	*Width (mm)*	*Cth(J/K)*	*Rth(K/W)*	*τ (s)*
Silicon, Die	13.55	0.375	13.55	0.1127	0.01334	0.0015
Solder	13.55	0.05	13.55	0.0135	$8.2523.10^{-3}$	0.0001
Copper, Cu	14.15	0.3	14.15	0.1935	0.039	0.0075
AIN	16.15	1	16.15	0.5681	0.0242	0.0137
Copper, Cu	16.75	0.3	16.75	0.2730	0.0028	0.0007
Solder	17.1	0.175	17.1	0.0731	0.0175	0.0012
Baseplate	27.1	5	27.1	5.446	0.0569	0.3098
Grease	27.2	0.05	27.2	0.0728	0.0678	0.0049

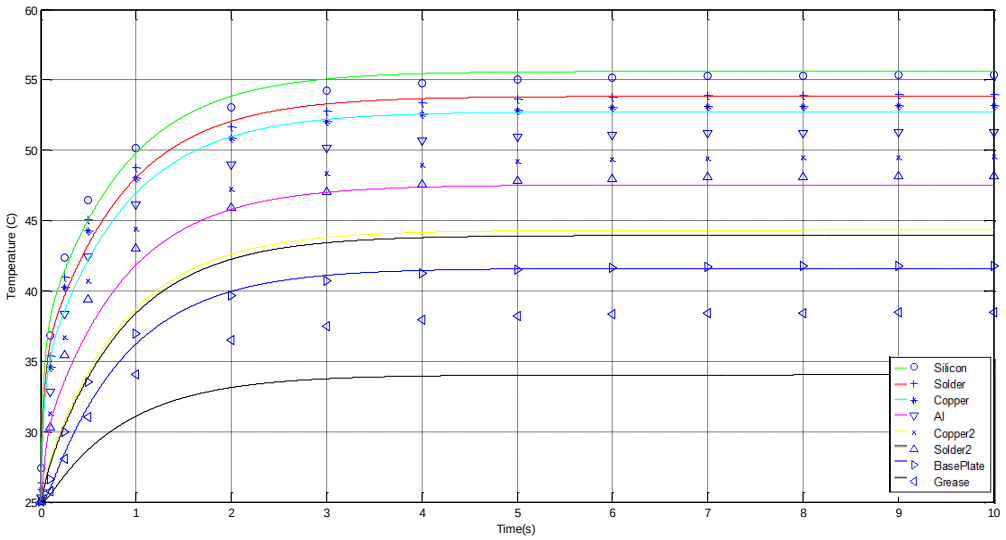


Figure 3.24 Temperature distributions over each layer by analytical solution vs FE results

As it is seen from Figure 3.24, when spreading angle analyses (coloured curves) are compared with FEM analysis (shaped curves), accurate results are obtained especially for the initial layers. Analytical derivation is acceptable for estimating junction (silicon), solder and baseplate temperatures although approximately 4°C difference is estimated for substrate and grease layers. The possible reason for the inaccuracies is related to the thickness of the direct bonded copper (DBC) substrates where it is stated that [235] spreading angle model with a 45 degrees assumption could provide less than 20% error of thermal resistance for a certain thickness range. Dimension dependent thermal impedance model with dynamic spreading angle assumption proposed by [69] and boundary condition

depended model proposed by [86] would increase the accuracy for the multi-chip power module where the chips are located near the edge of the substrate layers.

3.10 Thermal Modelling in Discrete Domain

In this section, discrete domain analysis was used to perform the proposed thermal model. The z-domain analysis advantages can be listed as follows:

- Increased computation speed
- Reduced order modelling
- Accurate thermal impedance matrix for multichip devices
- Applicable to dSPACE implementation for experimental verification (see section 4)

Forward Rectangular Euler's rule was applied to the thermal coefficients which were in s-domain. The transfer function *H(s),* equivalent to eqn. 3.21, can be expressed in discrete domain as:

$$H(s) = \frac{b}{s+a} \rightarrow H(z) = \frac{b}{\frac{z-1}{Ts}+a} \tag{3.34}$$

where T_s is the sample time. By recalling eqn. 3.21; applying a heat source, P_i, the change in the temperature, ΔT, can be expressed as follows:

$$\Delta T = \frac{1/C_{th}}{s+1/R_{th}C_{th}} P_i \tag{3.35}$$

This can be rearranged as in eqn. 3.36:

$$\Delta T = \frac{P_i}{sC_{th}} - \frac{\Delta T}{sR_{th}C_{th}} \tag{3.36}$$

Then, conversion from s-domain to z-domain can be written as (Please see the Appendix for extended derivation):

$$\Delta T = \frac{P_i}{C_{th}} \frac{1}{z-1} - \frac{\Delta T}{R_{th}C_{th}} \frac{1}{z-1} \tag{3.37}$$

Implemented simple thermal network stated in eqn. 3.37 is shown in Figure 3.25. The model generates one simple exponential term of RC network and is derived in Simulink.

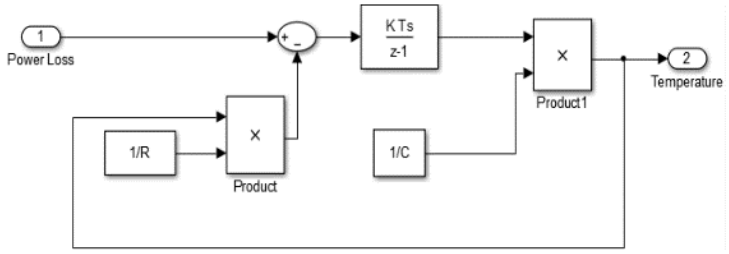
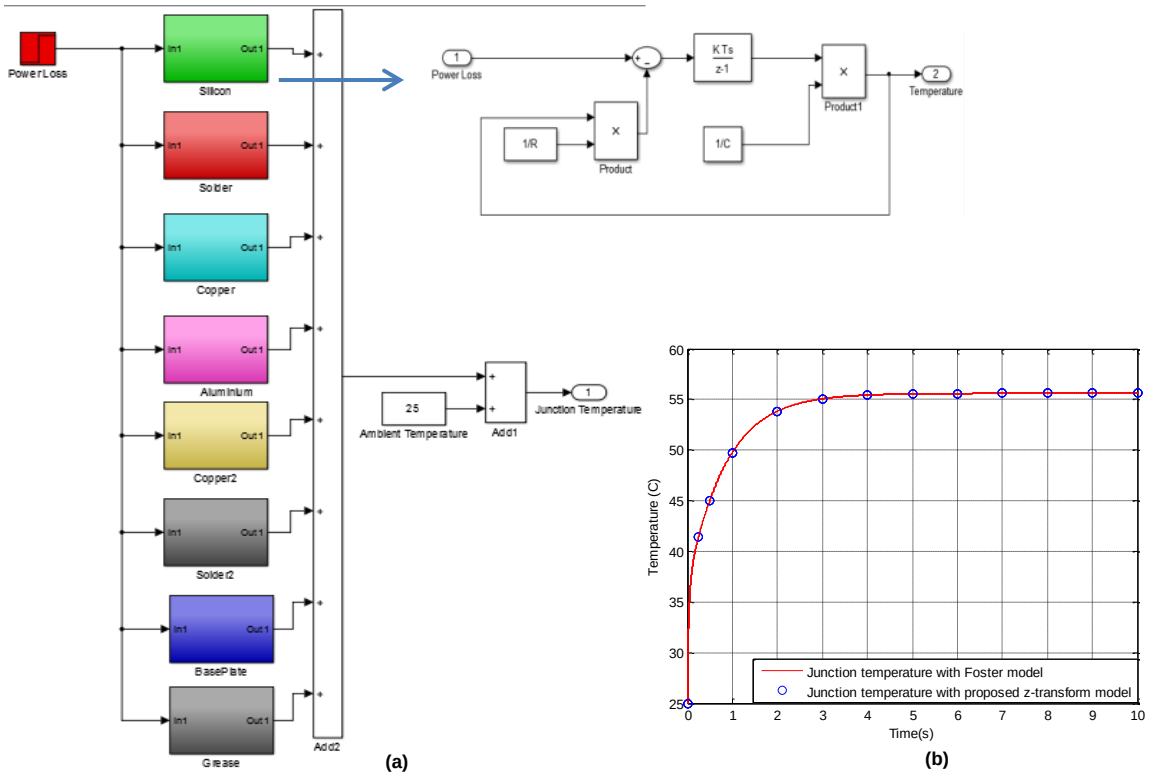


Figure 3.25: Simple Thermal Network model in Simulink

8th order Laplace form of RC network was implemented by using the thermal parameters extracted from transformation algorithm as shown in Figure 3.26 (a).



(a) **(b)**

Figure 3.26: 8th Order thermal model in discrete

Each block contains one single element of thermal model. Total temperature for each layer is added to ambient temperature which was selected as 25°C. Thermal parameters are analytically calculated based on the spreading angle effect (see Table 3.5) analysis, using the transformation algorithm from Cauer to Foster model with MATLAB coding. Then, two different modelling methods were simulated individually; First one with circuit elements as shown in Figure 3.17, and the proposed z-transform based model as shown Figure 3.26 (a).

Table 3.5: 8th Order thermal model in discrete

Layer	Thermal Identity (Foster)		
	Cth(J/K)	***Rth(K/W)***	***τ (s)***
Silicon, Die	6.709	$9.822.10^{-6}$	$6.59.10^{-5}$
Solder	$2.496.10^{9}$	$5.84.10^{-14}$	0.0001
Copper, Cu	0.2159	0.0065	0.0014
AIN	$6.84.10^{4}$	$3.2769.10^{-8}$	0.0022
Copper, Cu	10.2515	$3.0113.10^{-4}$	0.0030
Solder	0.4339	0.0189	0.0082
Baseplate	0.6576	0.0608	0.0399
Grease	5.894	0.1432	0.8440

Step input which represents 133.2 W heat sources was applied as input in both models. The junction temperature of conventional Foster and z-domain based proposed thermal models can be seen from Figure 3.26 (b). Good agreement is obtained between both models; hence, the proposed model is applicable to represent temperature, accurately.

Another example load profile was applied to the z-domain model using a regular square wave signal with amplitude 133.2 at 7.5 seconds sample time as shown in Figure 3.27 (a). Temperature estimations at heating and cooling stages of each are shown in Fig 3.27 (b) for each layer.

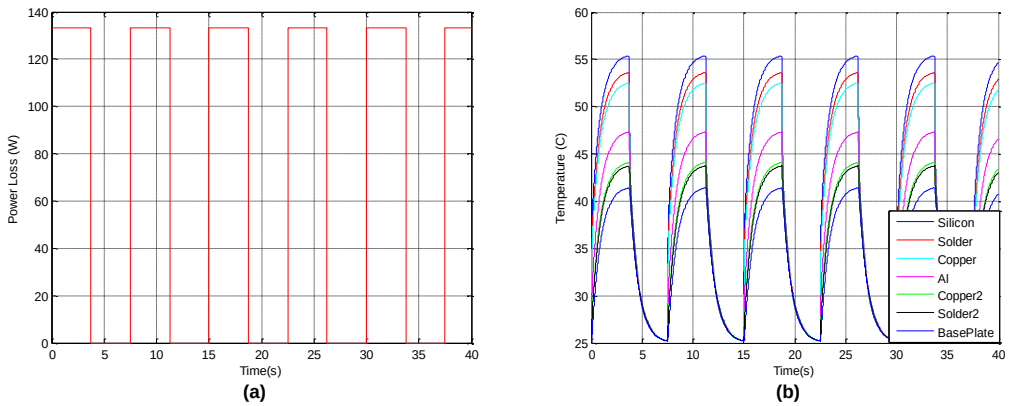


Figure 3.27 (a) Total Power Loss and (b) Temperature estimated for each layer

3.11 A 3D FE Model of Multichip Power Module

In order to detect cross coupling heat spread through module, 3D finite element model of the device was implemented using COMSOL Multi-physics software. The model is constructed based on the actual dimensions of the internal physical layers and material

properties supplied by producer. Heat Diffusion Equation is defined for the whole model to solve distribution of heat and temperature when an input heat power is applied. Identical boundary conditions were applied as in single chip FE model defined in Section 3.8. A 3D rectangular domain which represents the heat sink was attached to the rear surface of the base plate via a thermal grease layer for providing heat emission. It was modelled as a block with the recommended size in [229] (200mm x 300mm). Boundary condition was applied to the bottom surface of the heat sink as a constant cold plate at 25°C. The geometry was constructed with 313454 elements. The meshed view of the model is shown in Figure 3.28.

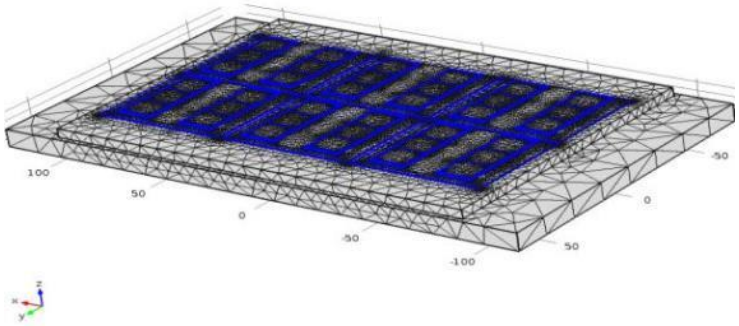


Figure 3.28 Meshed Model

Physical view of the module is shown in Figure 3.29. It is seen that the module has six legs; each consists of four IGBT and two diode chips. All chips are at the same size and with geometrical symmetries.

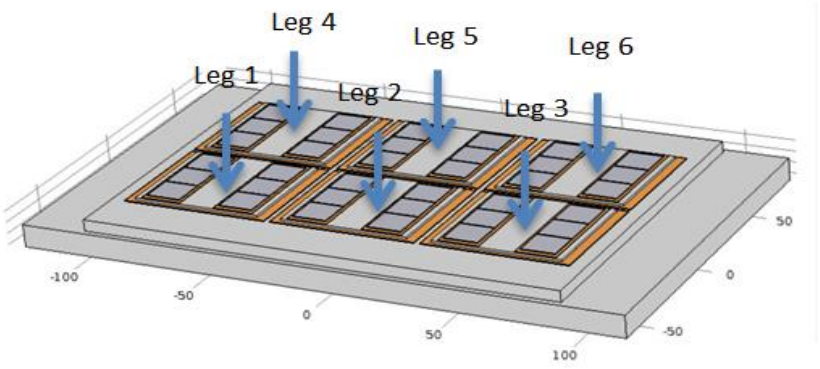


Figure 3.29 3D FEM of IGBT/Diode

Therefore, as an example, the heat flux distribution caused by chip DG33 is equal to heat flux distribution at UG11, UG33 and DG11 along different directions as shown in Figure

3.30. Hence, the circled chips were heated individually for thermal parameters extraction, only since all the other chips are in symmetry with them along different axes.

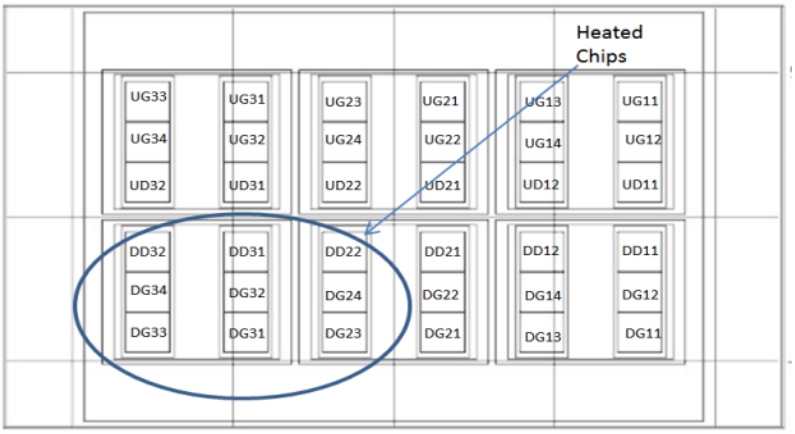


Figure 3.30 Overhead view of the model with entitled chips where UGs & DGs state upper and down IGBTs and UDs and DDs are the upper and down diodes, respectively

3.12 Operation of Thermal Impedance Matrix

The heat transfer analysis was further expanded for whole power module by taking consideration of heat coupling effects and temperature dependency of the power losses. This was achieved by implementing the thermal impedance matrix. For *M* layers and *n* heating sources, the temperature of each layer can be expressed as:

$$T_m(s) = \sum_{n=1}^{N} \sum_{k=1}^{Kmn} \frac{A_{mnk}}{s+\alpha_{mnk}} P_n(s) \tag{3.38}$$

where *A* is the coefficient $1/_{Cth}$ and α is the $1/\tau$ in eqn. 3.21. A matrix form of eqn. 3.38 can be derived as in eqn. 3.39 where a_1a_1, ... a_{MN} are the transfer functions of thermal impedances.

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jN} \\ T_{solder1} \\ \vdots \\ T_{AlNN} \\ \vdots \\ T_{baseplate} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1N} \\ a_{21} & a_{22} & \cdots & a_{2N} \\ & \vdots & \vdots & \\ a_{N1} & a_{N2} & \cdots & a_{NN} \\ & \vdots & & \\ & \vdots & & \\ & \vdots & & \\ a_{M1} & a_{M2} & & a_{MN} \end{bmatrix} \cdot \begin{bmatrix} P_{in1} \\ P_{in2} \\ \vdots \\ P_{inN} \end{bmatrix} + T_0 \tag{3.39}$$

The general thermal impedance implementing approach can be expressed in Figure 3.31 where the thermal characteristic was estimated in time domain, then formed in s-domain and implemented in z-domain.

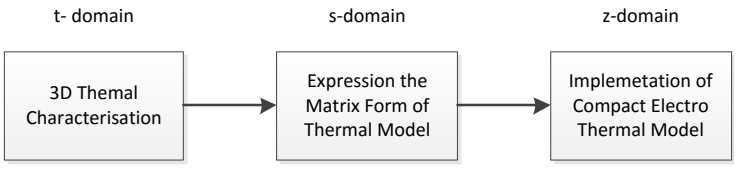


Figure 3.31 Process of Thermal Model Implementation

In order to extract the thermal characteristics of the whole module, each chip highlighted in Figure 3.30, was heated by a constant 133.2 W heat source in time domain based individual simulations. Simulation time step was set to 1 millisecond and it was computed until the step response of heating curve reaches steady state or thermal equilibrium. Individual chip heating operations for the DG33 and DD22 are shown in Figure 3.32 (a) & (b), respectively.

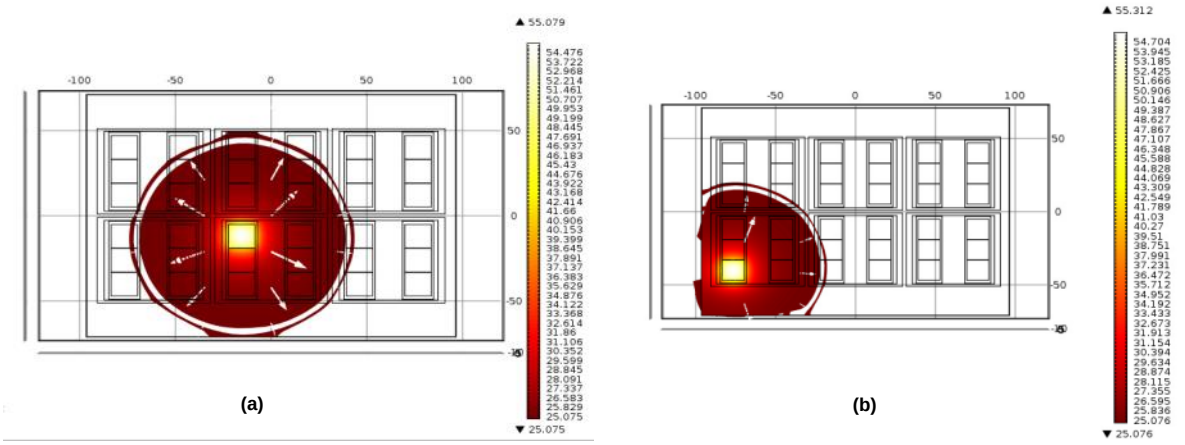


Figure 3.32 Heating operations for (a) DG33 and (b) DD22 with 133.2W heat source

The area of the effective heated region strongly depends on the location of the heat source. For example, when the chip DG33 is heated, only five neighbouring chips and the layers underneath are affected by heat coupling effects. However, the total affected region is wider when DD22 is heated individually. Hence, it is expected that the chips located in the middle will experience higher temperatures caused by cross coupling effects. Heat flux through both chips can be seen in Figure 3.33.

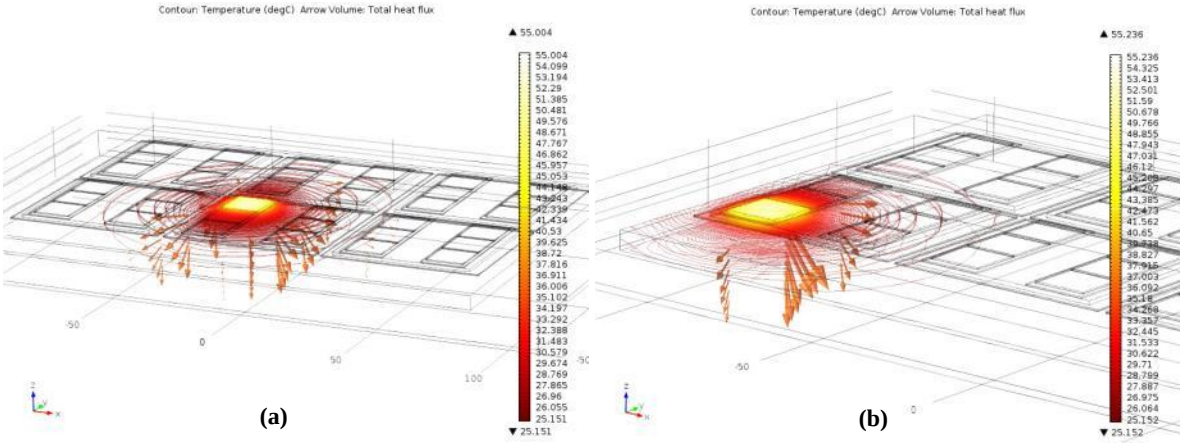


Figure 3.33: Heat Flux through DD22 (a) and DG33 (b) when133.2W heat source is applied

Example temperature distributions on chip DG33 due to its self-heating and coupling effects on the chip DG34 and the layers underneath are presented in Figure 3.34 (a) & (b), respectively. Approximately 7 °C temperature increment occurred on the chip DG34 due to the heat occurring on the DG33 as it was inclined from the initial 25 °C to 31.8 °C.

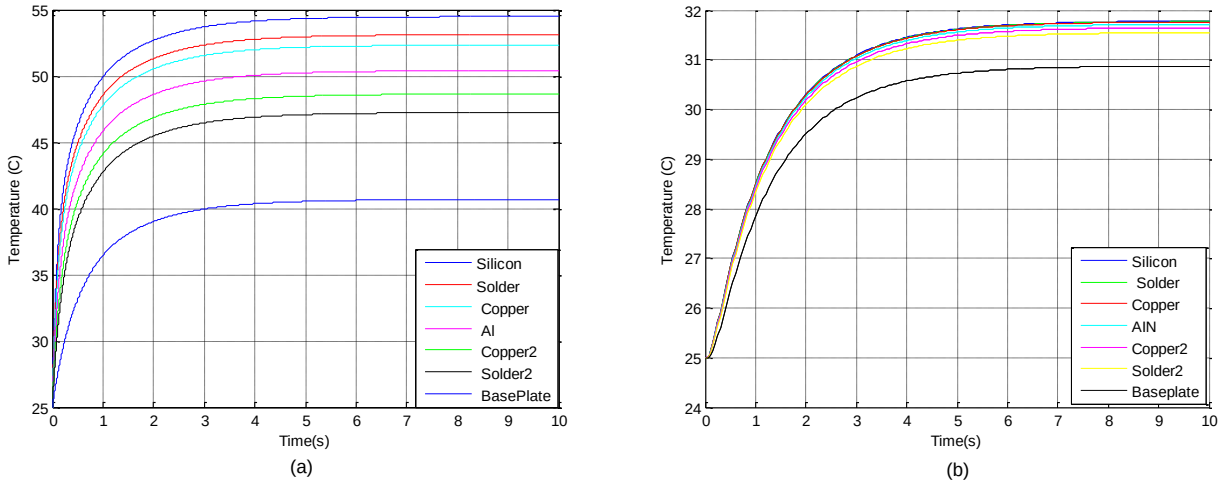


Figure 3.34 (a) Temperature estimations of DG33 and the layers underneath (due to self-heating) (b) Temperature estimations of DG33 and the layers underneath (due to heat coupling effect caused by heating DG34)

3.13 Thermal Impedance Extraction of Internal Layers

The generated heat curves found by using FE simulation are shown in Figure 3.35 along with the original 3D FEM model results. The extracted curves are represented as circles on the estimated temperatures of each layer. From the generated heat curves, coefficients R_{th} and C_{th} for each individual layer were extracted by curve fitting study using least square method.

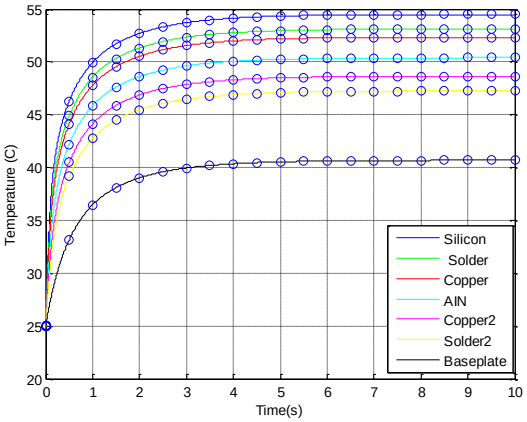


Figure 3.35 Temperatures of DG33 and layers underneath by FEM (self-heating of DG33) vs. fitted data by curve fitting

For more accuracy, the thermal impedance of each extracted curve was represented by three exponential terms. For instance, the coefficients *A* and *α* of eqn. 3.38 were calculated in order to define extracted thermal parameters for the Silicon Die chip, DG33, as follows:

$$R_1(s) = \frac{A_1}{s+12.953}\ ,\ R_2(s) = \frac{A_1}{s+0.822}\ ,\ R_3(s) = \frac{A_1}{s+2.8212} \qquad (3.40)$$

where A_1=1.127, A_2=0.057.4, A3=0.183 and time constants τ1=0.077s, τ2=1.215s and τ3=1.354s. The same process was applied for all the internal layers and the extracted parameters are shown in Table 3.6.

Table 3.6 Thermal Parameters for Chip DG33 and Layers underneath due to Self-Heating

Layer	Thermal Capacitance			Thermal Resistance		
	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$
Silicon, Die	0.887	17.53	5.45	0.0871	0.069	0.065
Solder	1.066	17.76	5.67	0.0785	0.068	0.063
Copper, Cu	1.187	17.91	5.81	0.0737	0.068	0.063
AlN	1.593	18.44	6.4	0.0634	0.066	0.060
Copper, Cu	2.147	19.16	7.27	0.0558	0.065	0.056
Solder	2.709	19.99	8.35	0.0513	0.062	0.052
Baseplate	7.177	18.32	641	0.051	0.062	0.003

Then, thermal parameters, which represent the coupling effects, were extracted using one exponential term and they are shown in Table 3.7. Previously developed Simulink model in Section 3.10 was updated with thermal blocks that represent the self-heating and heat coupling effects for each layer, similar to the parameters shown in Table 3.6 and 3.7.

Table 3.7 Thermal Parameters for Chip DG34 and Layers underneath due to Coupling Effect when DG33 is heated

Layer	Thermal Identity	
	C_{th}	R_{th}
Silicon, Die	23.074	0.0554
Solder	23.104	0.0553
Copper, Cu	23.144	0.0552
AIN	23.075	0.0549
Copper, Cu	23.568	0.0544
Solder	23.949	0.0537
Baseplate	26.8	0.0486

3.14 Implementation of Electro Thermal Model with Cross Coupling Effect

In order to design an electro thermal model for any semiconductor device, full description of current-voltage ratings, power loss characteristics and thermal behaviour of the device should be identified. The scheme of the developed electro thermal model with the power loss model is shown in Figure 3.36. The generated input current signal was combined with look up tables where energy losses are provided to the thermal model. The control scheme triggers the power loss calculation and the total dissipated power is integrated with the thermal model. Temperatures from this model are fed back into power loss model; hence continuous electro thermal analysis is obtained.

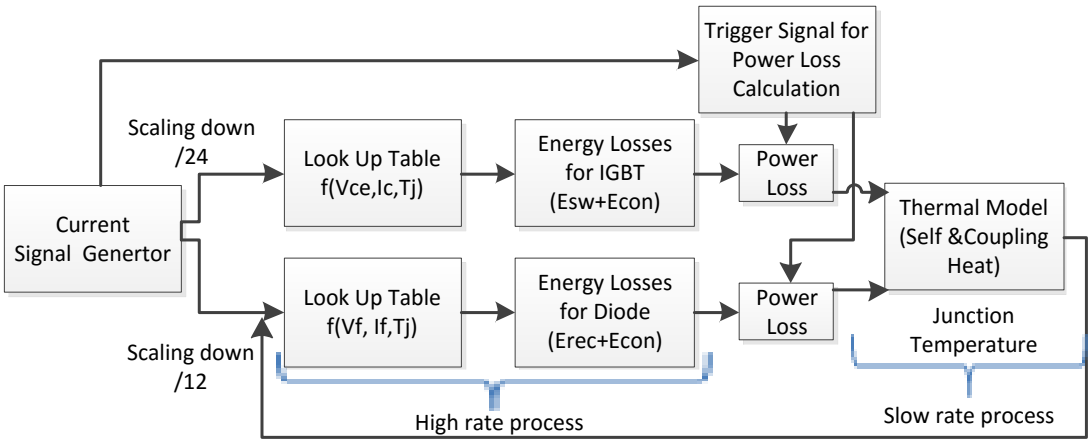


Figure 3.36 Schematic of the Developed Model in Simulink

A compact electro thermal model of the power module was developed based on z-domain analysis with Simulink. The electro thermal model of 1st leg of IGBT module can be seen

from the Figure 3.37. In the model, diodes (DD32 & DD31) are modelled in light grey where the IGBTs (DG31, DG32, DG33 & DG34) are modelled in bold grey blocks. The blocks include the thermal impedance of self-heating for the silicon chip and seven layers underneath and the thermal impedance of cross-coupling effects to the neighbour chips and layers. The green blocks are the power loss models for each individual chip.

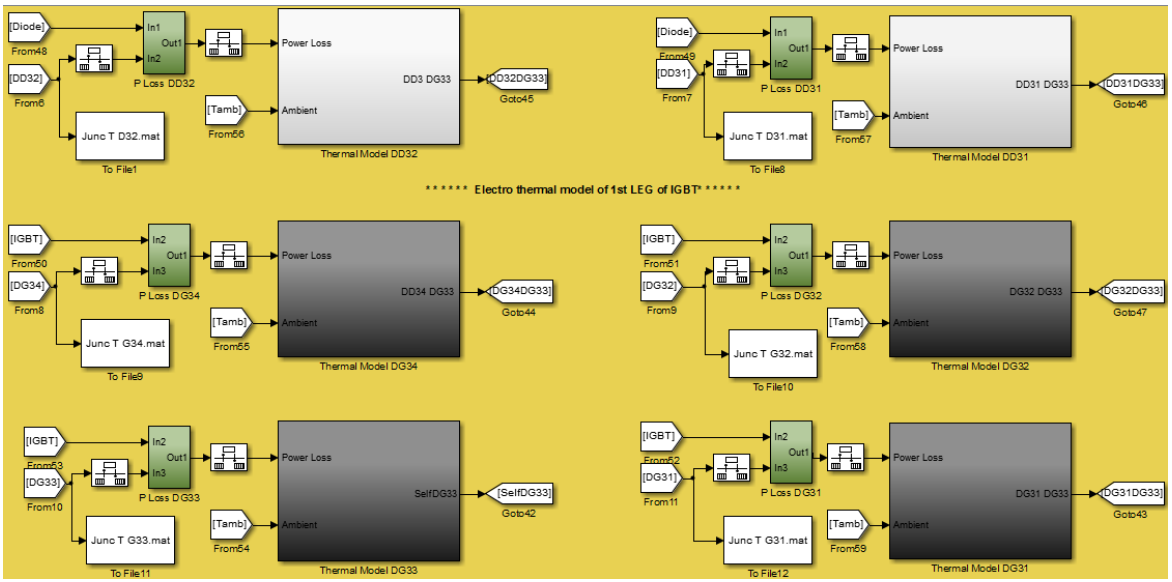


Figure 3.37 Electro thermal model of 1st leg of IGBT module

Sample blocks in each thermal model are shown in the Figure 3.38. Red block contains the thermal parameters extracted for self-heating and white blocks contain thermal parameters caused by coupling heat effect to neighbour layers when the selected chip is heated.

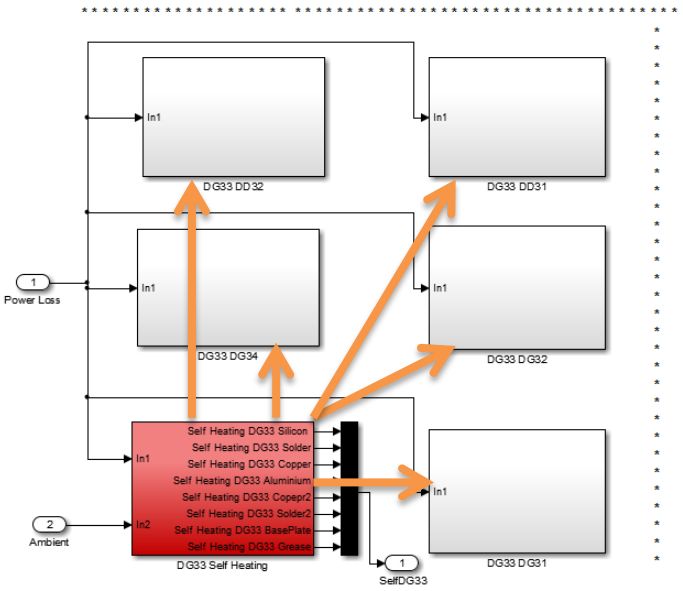


Figure 3.38 Heating operation of DG33 including cross coupling effects

Since heating operation of chip DG33 causes coupling heat effect on six neighbour layers, there are six thermal blocks around this chip containing the coupling effect thermal parameters. During simulation, each temperature is calculated at each single layer and they are fed back into individual power loss models. Figure 3.39 shows the model inside the block "ThermalModelDD31". It is seen from the model that when the diode chip DD31 is heated, temperature rises for DG33 and layers underneath are multiplexed and output from the block; then inserted to "Demultiplexing Block". The same procedure is applied in the other blocks on the 1st leg and temperature detection is completed by addition of temperature rise occurred in each layer.

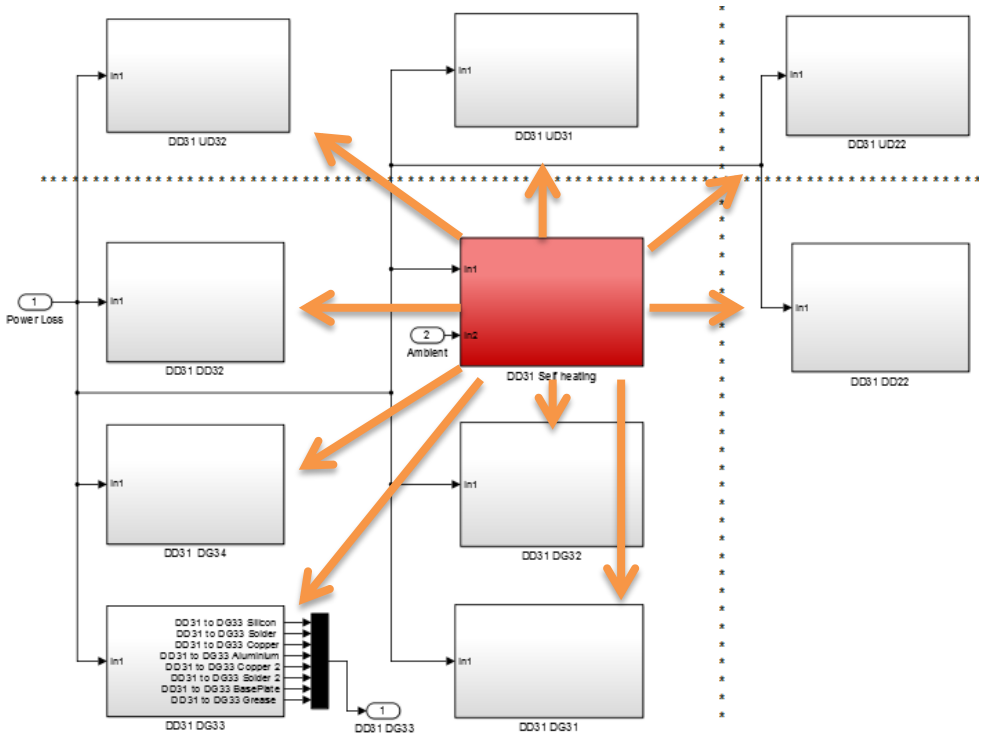


Figure 3.39 Heating operation of DG33 &Thermal Model including cross coupling effects

Note: The temperature processed only for DG33 and the layers underneath in the Figures 3.38 & 3.39. Hence, related signals are multiplexed and processed only for this chip. Estimations for other chip layers were removed in purpose for clarity and easy explanation.

3.15 Validation of the Simulink Model with FEM

In order to verify the electro thermal model; a test case was applied for both FEM and Simulink models by applying conduction losses, only. Switching loss calculation blocks were

removed in Simulink model and switching losses have not been considered in both simulations due to the FE solver speed limitations. The switching occurs in micro seconds for the power module; hence, it is computationally not convenient to be represented until the steady state temperature was reached in FE solver. A square wave input signal with 50 A amplitude, representing the maximum chip current for IGBT chips (see appendix), was used to represent the power loss for the thermal model. This signal was applied at switching frequency 20 Hz and with 50% duty cycle. On the other hand, 133.2 W heat losses were applied as initial heat source in FE model which are the associated total conduction power losses at 50 A current. Hence, same inputs were described for both simulations and the ambient temperature was set 25°C in both models. The power losses of the diode chip i.e. DD31, were calculated by the maximum diode current (100 A) in the model. Figure 3.40 shows comparison of estimated junction temperatures between FEM and Simulink.

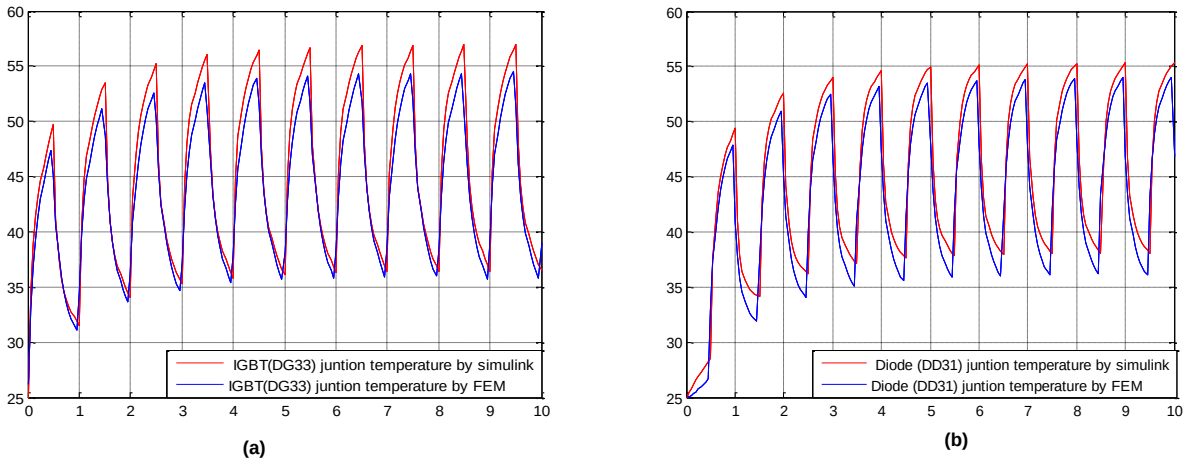


Figure 3.40 Junction temperature estimated with FEM and Simulink for (a) IGBT and (b) Diode chip

The maximum junction temperature difference between the FEM and Simulink model is approximately 2°C for the IGBT die. It is depicted that the temperature difference for the diode is higher than IGBT at cooling boundary. However, it is lower at the heating path which is around 1.8°C. The response speeds are also quite similar; therefore, good agreement in the estimated results is obtained between both models.

3.16 Implementation of Ideal Switching with Cross Coupling Heat Effect

Simulink model was further tested by generating pulse width modulation controlled current with 50% duty cycle at 25°C ambient temperature. In this case, switching loss calculation block was also considered and the total calculated power is automatically applied to the

thermal model at 1 kHz in a closed loop system. As it is seen from Figure 3.41 (a), when maximum allowed current 50 A passes through IGBT chip DG33, as an example, power losses are automatically calculated using lookup tables as function of the applied current, duty cycle and temperature estimates. The junction temperature estimates for this test reaches 81.2 °C.

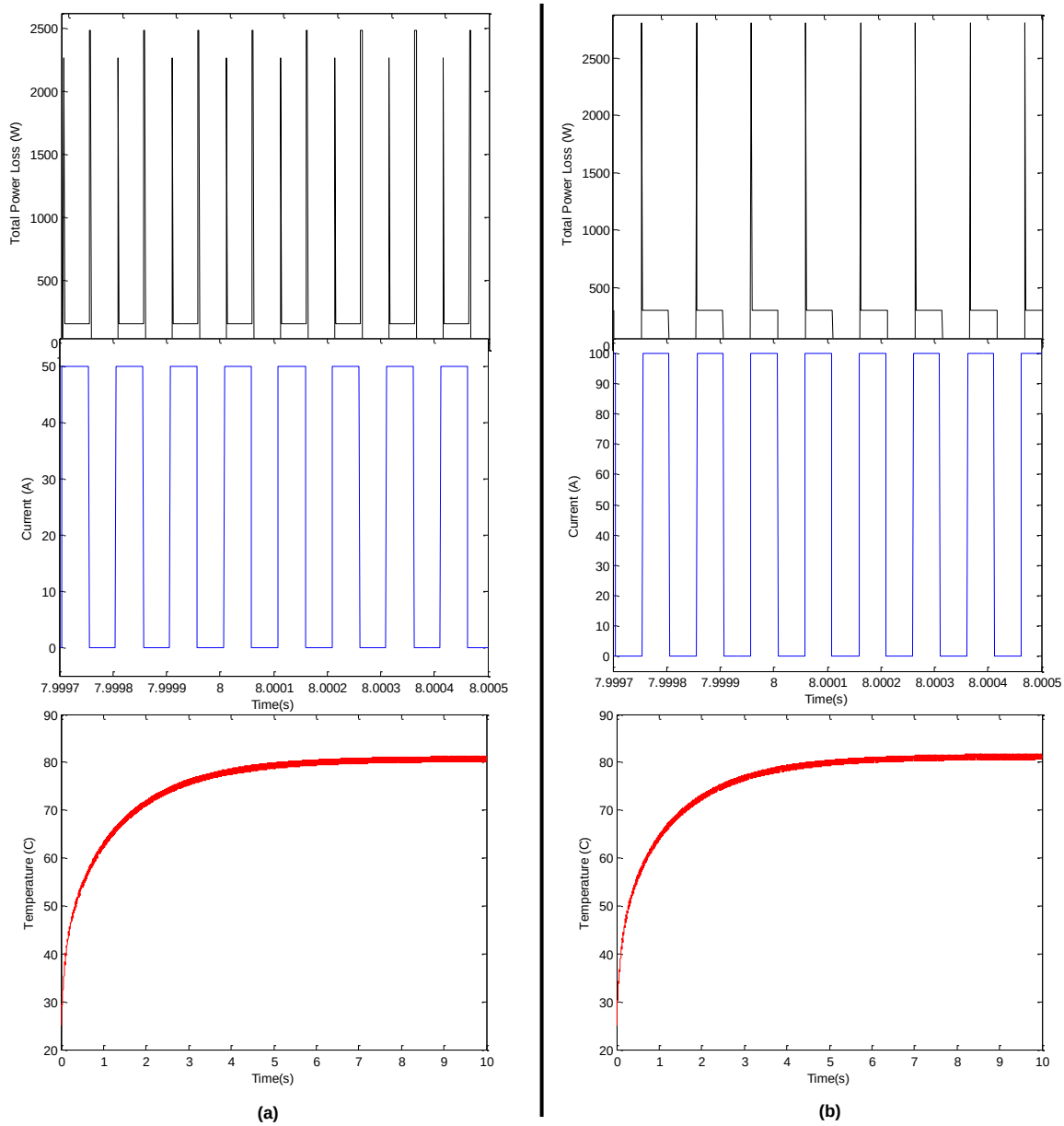


Figure 3.41 (a) Chip current vs. Power loss vs. Junction temperature of DG33 & (b) DD31

Switch on and off losses are calculated as 2.3 and 2.5 kW, respectively. The conduction loss is 190W when the device is conducting. On the other hand, the recovery losses for the diode can be estimated as 2.7 kW where the conduction losses are up to 310 W for the diode chip DD31, as it can be seen from the Figure 3.41 (b). The maximum junction temperature is also

reached up to 83.1 °C and approximately 2 °C difference is estimated compared to the IGBT chip DG33. The highest junction temperature was 91.3 °C for the DD22 diode. It can still be considered as safe region (~125°C) even for higher ambient temperatures (i.e. 40 °C).

3.17 Effect of the Cross Coupling Heat Effect

In order to detect the effect of the coupling heat effect, identical initial conditions were applied in the model; however, only self-heating based thermal impedance characteristics were considered. A case study is simulated that contains the self-heating thermal parameters for each chip and the layers underneath. The results can be seen in Figure 3.42.

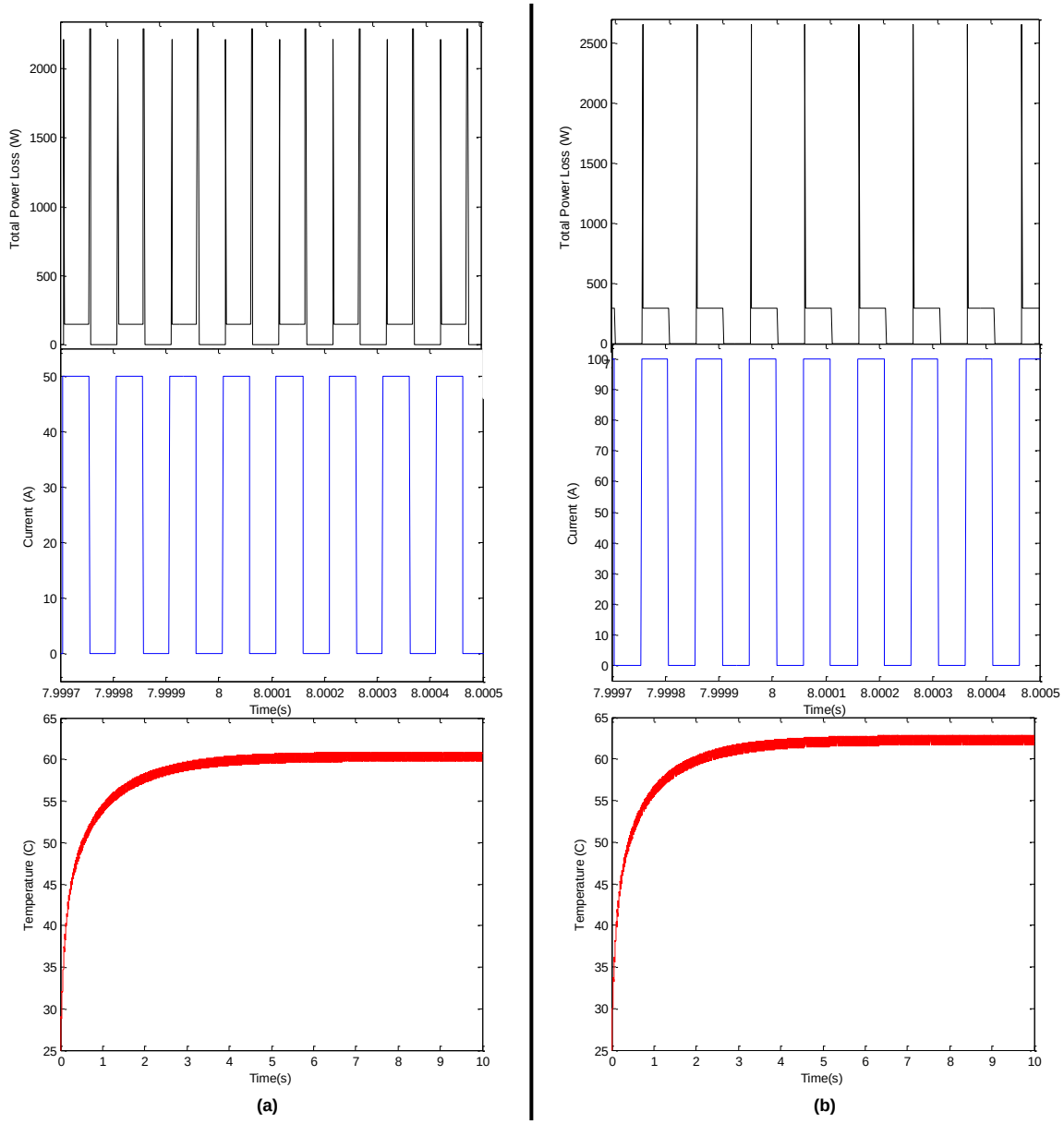


Figure 3.42 a) Chip current vs. Power loss vs. Junction temperature of DG33 & b) DD31

It is shown that the maximum junction temperature and total power losses are critically decreased if the cross coupling effect is ignored. The maximum junction temperature decreased from 81.2 °C to 60 °C for IGBT DG33 and 83.1 °C to 61.9 °C for the diode chip DD31. For both chips, the estimated temperature difference is around 20 °C which would cause serious degradation or faults, in case it is underestimated. Furthermore, regarding to the temperature difference, the maximum power losses for both chips also showed great difference between two cases due to the temperature depended power loss occurrences.

3.18 Effect of the Cooling Boundary Conditions

In previous sections, constant heat sink temperature (25 °C) was applied in the models as a boundary condition. This assumption was validated with the circuit implementation of Cauer and Foster networks and FE models. However, it can cause differences in the thermal impedance profile if the heat sink has floating (changing) temperature characteristics. The thermal impedance of the heat sink has considerable effect on the same characteristic of the each layer of the power module. In real-applications, this should be considered for accurate temperature monitoring. Therefore, a convection heat based cooling operation for the heat sink of the power module FE model is studied. The bottom boundary of the heat sink was modelled as a convection heating boundary and the heat transfer coefficient, h was assigned as 5 W/m^2K over this boundary representing natural convection. Similar to the previous sections 133.2 W constant heat source was applied to the top boundary of the chip DG33 and initial temperature was defined as 25 °C. All other material and dimension properties were identical with the previous models. Temperature distribution over the model and the convective heat flux at the bottom boundary of the heat sink can be seen in Figure 3.43 (a) & (b).

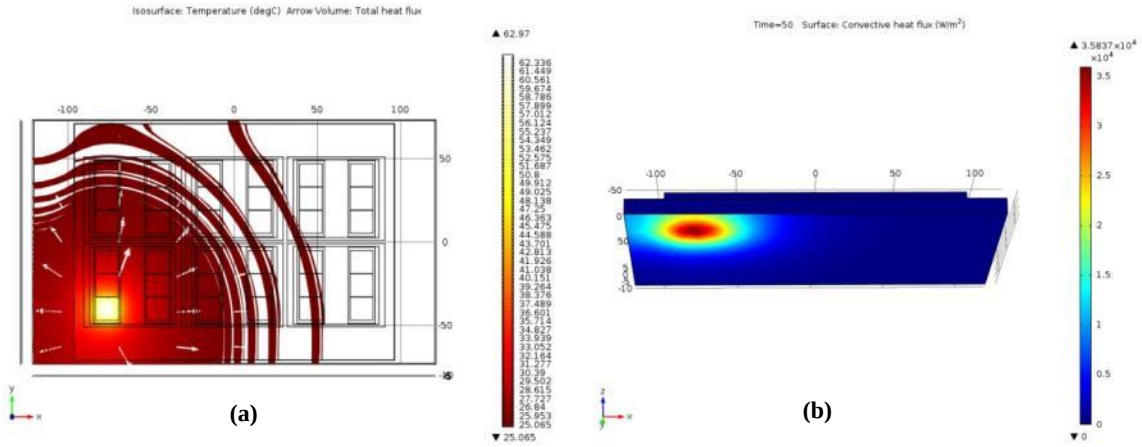


Figure 3.43 (a) Temperature estimation through different layers of the module when DG33 is heated (b) Convective Heat Flux through the bottom of the heat sink to ambient.

Temperatures of the each layer can be seen in Figure 3.44. It is seen that the silicon temperature is reached up to 62.3 °C where it was approximately 53°C for the constant heat sink temperature case.

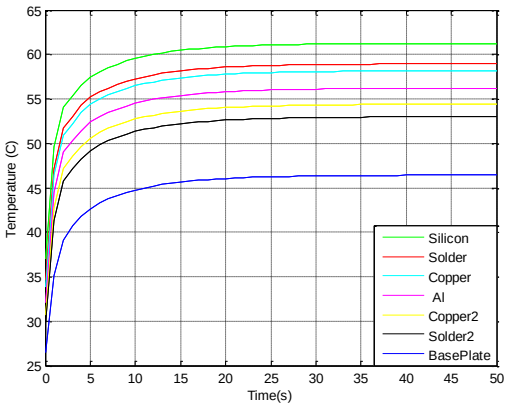


Figure 3.44 Temperature estimations for each layer

The steady state thermal equilibrium is also reached around 25th second, almost five times slower than constant heat sink temperature case. It is also seen that the total effective area of heat was larger than in the case when the heat sink temperature was constant; hence, the number of chips will be affected by increased cross coupling effect.

3.19 Real Time Electro Thermal Modelling for Insulated Gate Bipolar Transistors

Implemented model based mathematical electro thermal models in previous section are embedded in dSPACE real time system for validation purpose. In order to predict the temperature and power losses of four physically built boost converter units, experimental set ups were designed with three topologically different insulated gate bipolar transistors (IGBTs) and one with a SiC MOSFET device. In order to ensure that results are as accurate as possible environmental conditions of experimental tests were kept as identical with model based studies and thermal camera captures were taken for comparison purpose. The predicted power losses are subsequently used by FE models (derived in COMSOL) to estimate the heat distribution over the monitored modules.

Physically manufactured three different IGBT technologies are namely, punch through (PT), non-punch through (NPT) and field stop (FSTP) silicon trench gate technologies. PT device is structured by the replacement of the n+-substrate of the MOSFET with a p+-substrate, and an additional N+ layer which improves switching speed by reducing the number of excess holes that are injected into the P+ substrate [170]. On the other hand, NPT was generally made by using an N-doped substrate with the collector region grown on the backside. Since no buffer layer exists, this device has larger reverse voltage blocking capacity compared to the PT [165]. With the technological improvements in the gate structure, vertical, trench gate technology has been developed which allows even higher channel density by reducing the effective diameter of the gate and base region. It also reduces both conduction and switching losses compared to conventional PT and NPT structures [196]. Addition of a field-stop region to a thin-wafer NPT device enabled several further improvements in performance [169]. FSTP trench technology provides higher power density and optimized carrier concentration in the die. It can increase the carrier density in the vicinity of the trench gate which reduces substantially of the saturation voltage [154]. Moreover, the field stop layer accelerates the majority of carrier recombination during the turn-off time, and thereby, its tail current is much smaller than NPT or PT IGBTs which leads lower switching losses and lower turn-off energy. Figure 3.45 shows physical differences among these IGBTs.

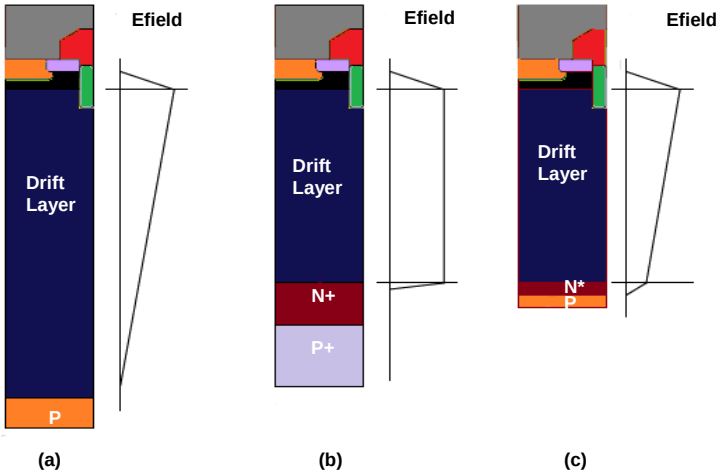


Figure 3.45 Trench NPT, (b) Trench PT and (c) Trench FS IGBTs

As it can be illustrated in Figure 3.45, the electric field shape is trapezoidal for PT, triangular for NPT, and FS has quasitriangular one [236]. Table 3.8 summarises important properties of IGBTs manufacturing technologies such as losses, field capacity and drift region thickness.

Table 3.8 Characteristics of three IGBT technologies [160], [226]

Property/Topology	Punch-Through (PT)	Non-Punch-Through (NPT)	Field Stop (FSTP)
E-field	punches trough drift region to buffer-shortens tail current	dissipates in drift region - lengthens tail current- raises E_{off}	punches through drift region to buffer-shortens tail current
Drift Region	Thin-lowers Vce(sat)	Thick -raises Vce(sat)	Thinnest - lowest Vce(sat)
Epitaxial Layer	Expensive-grown on p+ substrate	Injection layer realized by ion implantation- no epitaxial layer.	No epitaxial layer- Wafers as thin as 80um
Switching Losses	Low-short tail current, significant increase in Eoff with temperature	Medium- low tail current, moderate increase in Eoff with temperature	Low-short tail current, moderate increase in Eoff with temperature
Conduction Losses	Low-Vce slightly decreases with temperature	Medium-Vce increases with temperature	Low-Increases with temperature
Paralleling	Difficult-Must sort on Vce(sat), must share heatsink	Easy-Optional sorting, Recommend sharing heatsink	Optional sorting, Recommend sharing heatsink
Short Circuit Rated	Limited-High Gain	Yes	Yes
Vce Temperature Coeff.	Negative	Positive	Positive

3.20 DC/DC Boost Converter

DC-DC converters are electronic devices used for changing the DC electrical power efficiently from one voltage level to another. Boost converter or step-up converter is a power converter with a regulated output DC voltage greater than its input DC voltage. The ideal boost converter components are the switching device (IGBT, MOSFET), a power diode, an inductor and input/ output ripple capacitors. The circuit diagram of this converter can be seen in Figure 3.46.

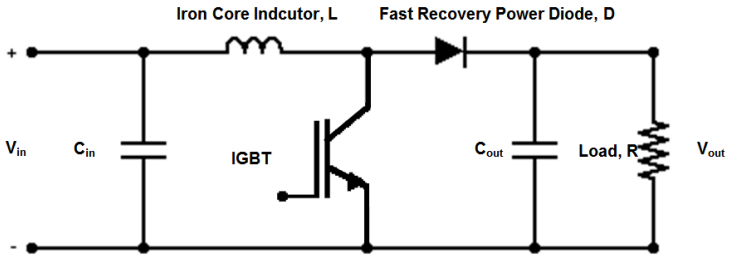


Figure 3.46 Boost Converter circuit

The on time of the switching device is a fraction of its time, T_p such that T_{ON}=DT, where *D* is the duty cycle. When the switch is in on position; the circuit is separated into two parts. These parts are on the left; the source is charging the inductor while the capacitor, which is on the right, maintains the output voltage using previously stored energy. When the switch changes its position into off-state, both DC source and energy stored in the inductor will supply power to the circuit on the right which boosts the output voltage. The output voltage can be maintained at desired level by controlling the switching time sequence which can be calculated as:

$$T_{ON} + T_{OFF} = T_P = 1/f \tag{3.41}$$

where *f* is the switching frequency.

$$T_{ON} = DT_P \,,\; T_{OFF} = (1-D)T_P \tag{3.42 \& 3.43}$$

Considering ideal components, when switch is turned on, voltage applied on inductor is;

$$L\frac{di_{in}}{dt} = V_I = L\frac{\Delta i_{in}}{DT_P} \tag{3.44}$$

Where *L* is the inductance; when switch is off:

$$L\frac{di_{in}}{dt} = V_I - V_O = L\frac{\Delta i_{in}}{(1-D)T_P} \tag{3.45}$$

By equating eqns. 3.44 and 3.45, following equation is obtained;

$$\frac{DT_P V_I}{L} = -\frac{(1-D)T_P}{L}(V_I - V_O) \tag{3.46}$$

Simplifying the eqn. 3.46;

$$V_I = (1-D)V_O \tag{3.47}$$

∴ for a lossless system input power (P_i) is equal to the output power (P_o)

$$P_{in} = P_{out} = I_{in}\, V_I = I_o V_o \tag{3.48}$$

$$I_o = (1-D)I_I \tag{3.49}$$

Current signal characteristics of components during switching can be seen in Figure 3.47.

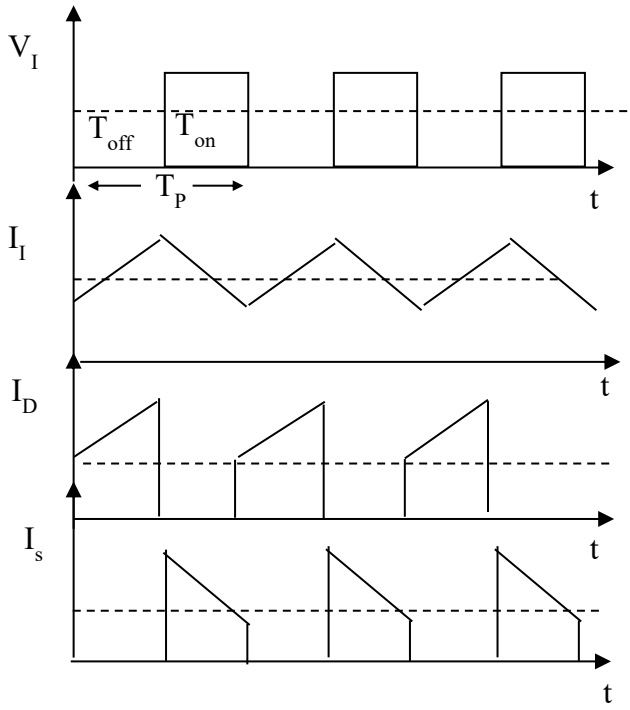


Figure 3.47 Current Signal Characteristics

3.21 Physical Boost Converter design

Four physical boost converters were built using identical blocking and storing components but with different switching element technologies. Converter parameter specifications are listed in Table 3.9.

Table 3.9 Boost Converter parameter specifications

Element	V_{in}	IGBTs	MOSFET	Diode	S. Freq.	Duty	Inductor, L	C_{in}, C_{out}
Values	5-70 V	600/15A	1200/15A	300/20A	5-150 kHz	50%	1mH/12A	82µF/450V

3.21.1 Switching Devices

Selected IGBT components are commercially available; TO-220 are packaged, and they are all from different manufacturers. The NPT IGBT is the NGTB15N60S1EG from On Semiconductor, PT one is the STGP14NC60KD from ST Microelectronics and FS is the IKP10N60T by Infineon. Each device has approximately equal power loss profiles at 25°C and they are purposely selected based on their similar current ratings. The characteristics of selected devices are shown in Table 3.10:

Table 3.10 Si IGBTs and SiC MOSFET specifications

IGBT (A)	IGBT (B)	IGBT (C)	MOSFET	Unit
NPT-Si-Trench	PT-Si- Trench	FSTP-Si-Trench	SiC-Planar	-
Cost: 1.00	Cost:1.2	Cost: 1.19	Cost: 11.52	£
V_{CEs}: 600	V_{CEs} 600	V_{CEs}: 600	V_{DSs}: 1200	V
$I_{C\ (T=25C)}$: 25	$I_{C\ (T=25C)}$: 25	$I_{C\ (T=25C)}$: 20	$I_{D\ (T=25C):}$ 24	A
$I_{C\ (T=100C)}$: 15	$I_{C\ (T=100C)}$: 14	$I_{C\ (T=100C)}$: 10	$I_{D\ (T=100C)}$: 10	A
C_{ies}:1950	C_{ies}:760	C_{ies} : 551	C_{iis}: 667	pF
C_{oes}: 70	C_{oes}: 86	C_{oes}: 40	C_{oss}: 27	pF
C_{res}: 42	C_{res}: 15.5	C_{res}: 17	C_{rss}: 5	pF
Q_g: 88	Q_g: 34.4	Q_g: 62	Q_g: 36	nC
$t_{d(on)\ (T=25C)}$: 65	$t_{d(on)\ (T=25C)}$: 22.5	$t_{d(on)\ (T=25C)}$: 12	$t_{d(on)\ (T=25C)}$:19	ns
t_r: 28	t_r: 8.5	t_r: 8	t_r: 19	ns
$t_{d(off)}$: 170	$t_{d(off)}$: 116	$t_{d(off)}$: 215	$t_{d(off)}$: 47	ns
t_f: 140	t_f: 75	t_f:38	t_f: 29	ns
$E_{on\ (T=25C)}$: 0.55	$E_{on\ (T=25C)}$: 0.082	$E_{on\ (T=25C)}$: 0.16	$E_{on\ (T=25C)}$: 0.057	mJ
$E_{off\ (T=25C)}$: 0.35	$E_{off\ (T=25C)}$: 0.155	$E_{off\ (T=25C)}$: 0.27	$E_{off\ (T=25C)}$: 0.02	mJ
$P_{loss(T=25C)}$: 117	$P_{loss(T=25C)}$: 112	$P_{loss(T=25C)}$: 110	$P_{loss(T=25C)}$: 108	W

Physical view of a boost converter can be seen in Figure 3.48.

Figure 3.48 Physical view of a boost converter

3.21.2 Inductor

In order to decrease saturation of current flow even at high ratings, an iron-core type inductor with 1mH rating, manufactured by EPCOS, has been used. This type of the inductor is favourable because of its high saturation flux density.

3.21.3 Power Diode

An identical fast recovery diode was used for each boost converter unit. It is DPG 10 I 300PA by IXYS. The device has particularly short recovery time and low leakage current which would increase the total efficiency performance.

3.21.4 Capacitors

Input and output capacitors are Aluminium Electrolytic type and cylindrically manufactured by Panasonic. In order to limit the ripple of input and output voltages to their 2% for the frequencies between 10 to 100 kHz, 82uF input and output capacitors are selected. Input and output voltage readings were measured over these components, respectively.

3.22 Driver Unit Design

Switching elements have particular gate signal power requirements to turn on and turn off. A gate driver is essential for translating the low power TTL or CMOS logic signal, generated by signal generator units or controller ICs, to a higher voltage and higher current signals for rapidly switching the gate of the IGBTs and MOSFET. In other words, a gate driver is a power amplifier which can be provided either on-chip or as a discrete module. There are commercially available gate drivers for single switching devices or for power modules with multi-chip design. In this research, the gate driver circuit for DC/DC boost converter and DC/AC inverter were implemented by the author. In order to isolate low power switching signal and high power converter circuit, an opt coupler was embedded with a driver PIC for providing appropriate gate signal in terms of power level.

3.22.1 Optical Coupler

In order to obtain an adequate isolation between high power boost converter and more expensive signal generating unit (dSPACE), an opt-coupler chip was used in the configuration before enabling the driver chip. The opt-coupler package is the HCPL-4502/3 by Agilent Technologies configuration can be seen in Figure 3.49.

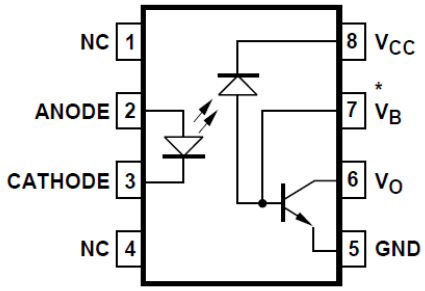


Figure 3.49 Configuration of the Opt coupler [237]

It is shown that there is an electrical isolation between LED and a photo detector. This transition isolates the driver and the converter protects the driver unit from any high current reversed from the converter. The photo-detector senses the light energy which is the converted form of the electrical signal by the LED. Then, this energy is converted it back to electrical signal by an amplification circuit at the output. The other important function of opt coupler is the filtering of the noisy signal.

3.22.2 Driver

The output signal from the opt coupler is embedded into the driver chip which can provide sufficient current and voltage level for the switching transient of the IGBT and MOSFET. TD351 by ST Microelectronics was purposely selected because of its inverting and non-inverting output features. The original gate signal is inverted during the isolation part in the opt coupler. Therefore, it has to be inverted back by the driver for determining on and off stages of the PWM signal correctly. The circuit configuration of the TD351 can be seen in the Figure 3.50. In order to decrease the voltage spike on the gate, the Miller clamp function is used and the gate output signal is constantly connected back to CLAMP pin for Miller Active Clamp function. Also, similar to opt coupler, a capacitor is connected closely to the VH and VL pins for ripple filtering.

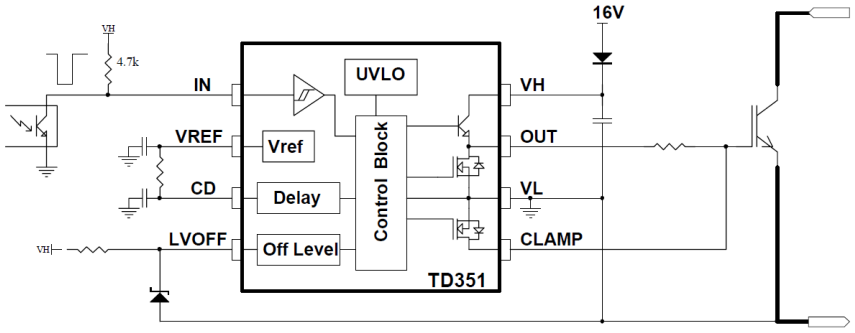


Figure 3.50 Configuration of the Opt coupler [238, p. 351]

3.23 dSPACE Real Time System

dSPACE Real Time system, available in Advanced Industrial Diagnostics Lab, was comprehensively used in this research for experimental validation of the modelling sections. dSPACE system is a powerful tool for prototyping, target implementation, and electronic control unit (ECU) testing. The dSPACE Control Desk Software was used for executing Real-Time Interface to Simulink which is a part of Rapid Control Prototyping and Hardware in the Loop (RCP and HIL) software. The platform is suitable for embedding Simulink models in Control Desk and it is able to record and export the experimental data in real time. Instead of using generic input signals in Simulink models, experimental data can be embedded within this platform and continuous execution of the models can be obtained. For instance, collector current and voltage of IGBTs are embedded into electro thermal models derived from Simulink to monitor real time power loss and temperature data in Control Desk.

3.23.1 Real time Platform

Real time interface (RTI) is the package needed for implementing Simulink models in dSPACE. These models are first converted into suitable C/C++ codes, and then they can be embedded in Control Desk via RTI. The platform is called DS1006 and it is the hardware platform where the complied script files are executed. It contains three key components: hardware, a code-development assistant, and a graphical user interface (GUI) which transfers the code onto the processor and monitors the execution of the program.

3.23.2 DS1006

DS1006 platform consists of a high-speed hardware processor, analogue and digital input-output (I/O) devices or interfaces, and a communication arrangement between the host computer and the platform. It is designed for calculating complex, precisely detailed simulation models that require enormous computing power and it is directly connectable to all dSPACE I/O boards via peripheral high speed (PHS) bus. The communication between the host computer and the modular system is through an optical cable. Physical view of the I/O platform and the DS1006 are shown in Figure 3.51 (a) & (b), respectively.

(a) (b)

Figure 3.51 (a) I/O Platform (b) DS1006 [239]

Features of the DS1006 board can be listed as:

- ✓ x86 processor technology x86-compatible 64-bit server multi-core processor
- ✓ Quad-Core AMD Opteron™ processor
- ✓ 512 kB L2 cache per core and 6 MB shared L3 cache
- ✓ 1 GB local memory for executing real-time models
- ✓ 128 MB global memory per core for exchanging data with the host PC
- ✓ Fully programmable from Simulink
- ✓ High-speed connection to all dSPACE I/O boards via PHS bus
- ✓ Multiprocessor system of several DS1006 processor boards via fiber-optic connection.

The platform also has multi I/O board, DS2201, for analogue to digital conversion. dSPACE I/O board is selected during start-up of the Simulink from the RTI block library which contains ports for all the peripherals available on the modular system and then attaches via Simulink. The block diagram of the DS1006 is shown in Figure 3.52.

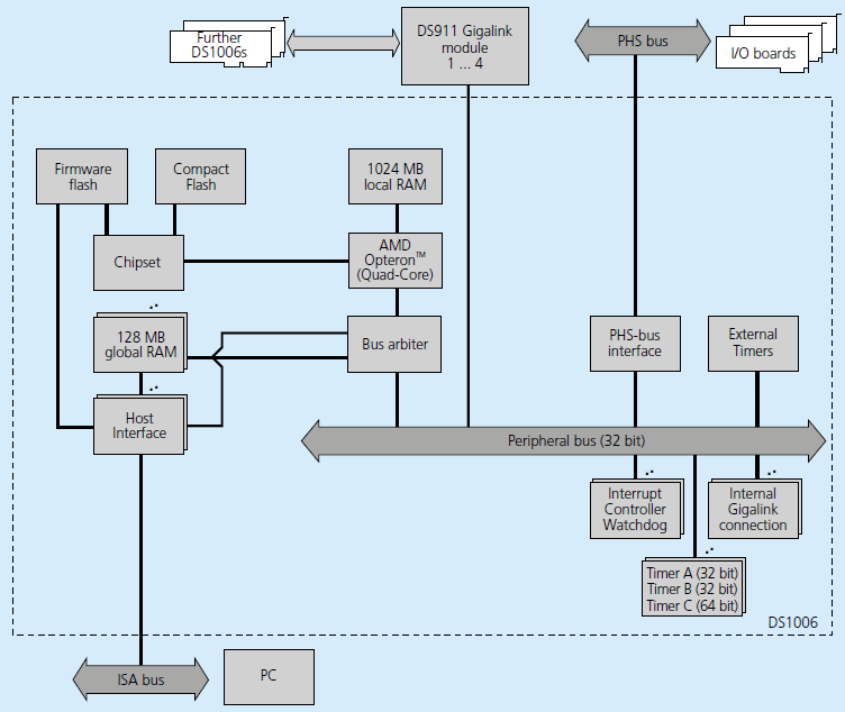


Figure 3.52 Block diagram of DS1006 [239]

Two additional boards also exist within the dSPACE system. The DS5101 for digital waveform output and DS 2004 A/D for digital-to-analogue conversion.

3.23.3 DS5101

DS5101 is a digital waveform output board for generating a multiple signals at various frequencies, such as incremental encoder signals and pulse-width modulation (PWM) waveforms. PWM is required in almost any control application. The features of this board can be listed as follows:

- TTL pulse patterns on up to 16 channels
- 25 ns time resolution
- 1-phase PWM
- 3-phase PWM
- 3-phase/6-channel PWM (includes converted signals)
- Incremental sensor simulation
- Monoflop signal generation

Physical view of the DS5101 is shown in Figure 3.53.

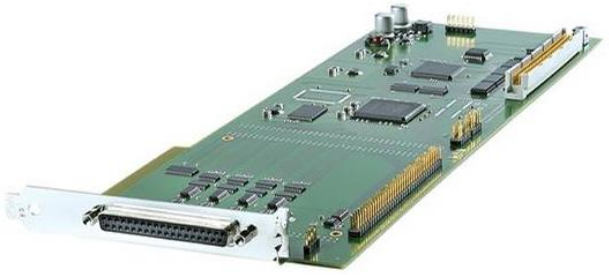


Figure 3.53 DS5101

3.23.4 DS2004

DS 2004 A/D Board is an analogue to digital conversion platform for digitizing input signals at high sample rates. It is also equipped with differential inputs and four triggers inputs for connecting to external trigger sources. It provides many different hardware- and software-based trigger mechanisms as well as data buffers for burst data transfer. The burst mode offers two ways of converting measurements; namely automatic continuous sample mode and triggered sample mode which is controlled by the software or a trigger event. The key features of DS2004 can be listed as follows:

- 16-bit independent A/D converters
- 16-bit resolution
- 800 ns conversion time
- ±5 V or ±10 V input voltage range
- 4 external trigger input lines
- total harmonic distortion (THD) ≤-85 dB (at 10 kHz, 10 V range)
  ≤-83 dB (at 10 kHz, 5 V range)

Physical view of the DS2004 board is shown in Figure 3.54.

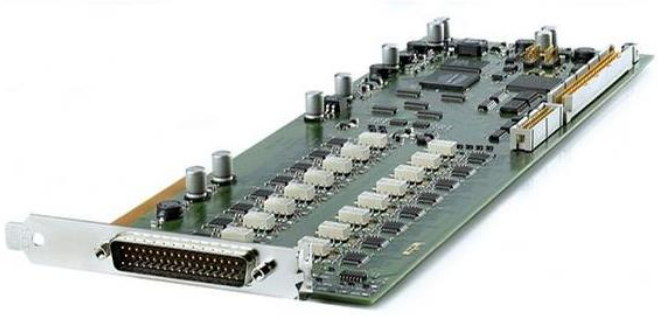


Figure 3.54 DS2004

3.24 System Design

The gate signals for each switching device located in boost converters were generated using dSPACE DS5101 digital to analogue converter card. Then power levels of these signals were increased by previously implemented driver circuit. In order to calculate the power loss and temperature profile of each IGBT, the collector current signals were monitored by hall-effect based ACS712 linear current sensors by Allegro Microsystems. The sensor is applicable for AC and DC current sensing in industrial systems with 185 mV/A output sensitivity. Configuration of the sensor can be seen in Figure 3.55.

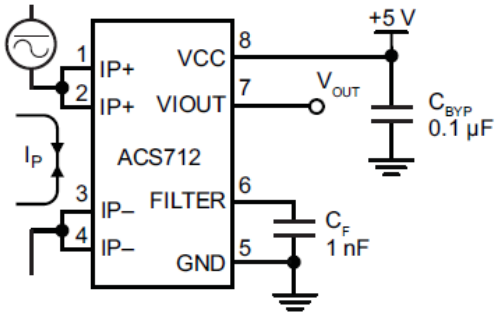


Figure 3.55 ACS712 Configurations [240, p. 71]

The ACS712 outputs an analogue signal, V_{OUT}. It can vary linearly with the uni- or bi-directional AC or DC primary sampled current, I_P. Filter capacitor, $C_{F,}$ is needed for noise management through ground. Collector to emitter current of the IGBTs is captured by ADC DS2004 as voltage ratings are calibrated in Simulink block for current equivalences based on the specifications stated in manufacturer datasheet. On the other hand, collector to emitter voltage is also directly captured by a voltage divider circuit, implemented with serially connected 1 MΩ resistors, and interpolated for associated saturation voltage level within look up tables. Boost converter units were operated in a temperature controlled chamber for controlling ambient temperature. View of experimental setup is shown in Figure 3.56.

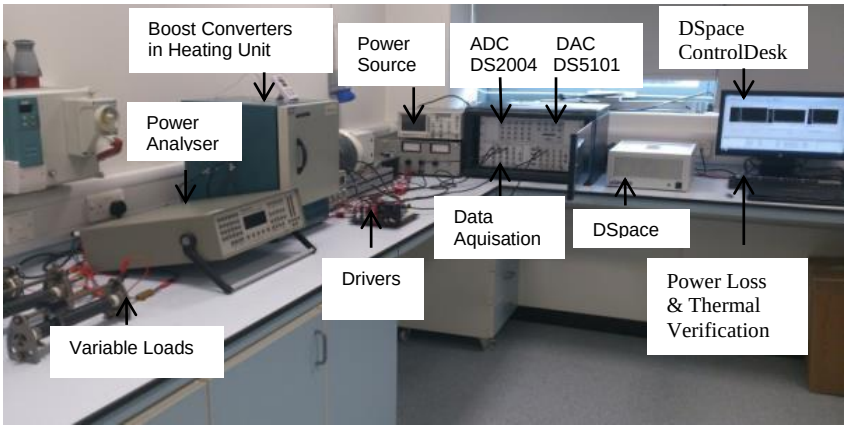


Figure 3.56 Experimental Set-up

3.25 Methodology

In order to extract the thermal parameters, each IGBT was initially supplied by a constant gate signal and 5V of collector-emitter voltage under 10 Ω parallel load conditions. Each device was operated until reaching to a steady state temperature. During the test, temperatures were captured by FLIR T440 thermal camera in every 5 seconds. It has a frame rate 60 Hz and a thermal resolution of 76,800 pixels. Output power of the boost converters were monitored by Voltech PM300A power analyzer. IGBT based boost converters were operated in this part of the study. SiC MOSFET based boost converters are examined in and performance comparison between Si IGBT is presented. The flowchart of the developed methodology and the experimental setup are shown in Figures 3.57 & 3.58.

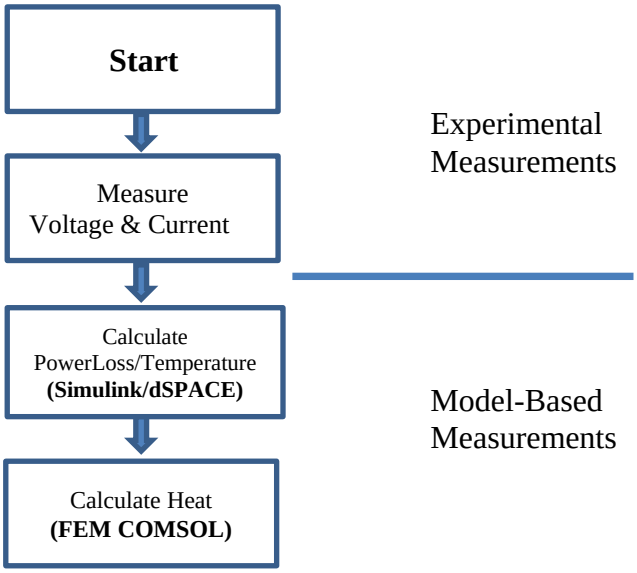


Figure 3.57: Flowchart of the proposed system

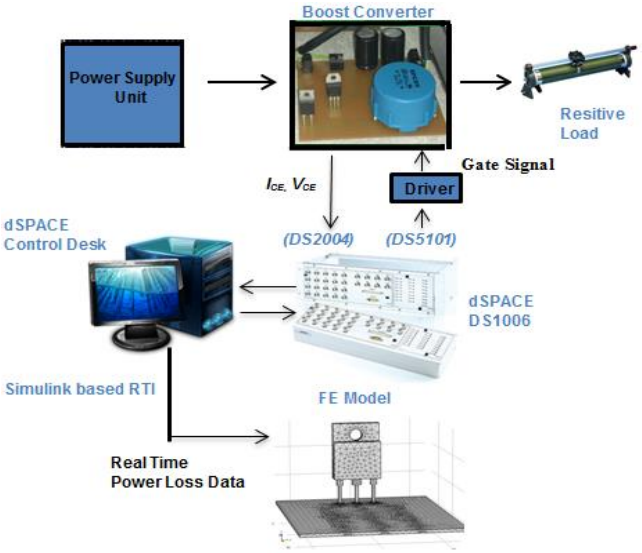


Figure 3.58: Schematic diagram of the proposed system

Device thermal resistance (R_{th}) and capacitances (C_{th}) were determined using eqns. 3.24 & 3.25. The calculated thermal resistances and capacitances are shown in Table 3.11. Then, the thermal model was built upon the discrete domain based modelling approach. In addition to the calculated thermal resistances and capacitances, measured currents and voltages are interfaced to the real-time electro-thermal monitoring scheme (implemented in dSPACE) depicted in Figure 3.59.

Table 3.11 Interpolated thermal characteristic

Tested Device	Thermal Capacitance			Thermal Resistance		
	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$
FS	0.22	0.02	0.0013	0.2911	0.409	0.5008
PT	0.24	0.015	0.019	0.282	0.35	0.502
NPT	0.28	0.018	0.0014	0.2811	0.4	0.5019

The dSPACE blocks are shown in Figure 3.59, two (DS2004ADC) blocks are used for current and voltage readings and three blocks (DS5101PWMDAC) are used for providing gate signals to each IGBT used in boost converters. A zoomed in view of power loss calculation blocks is illustrated in Figure 3.60. The output temperatures then fed back into power loss model along with the voltage and current signals for continuous monitoring of the electro thermal behaviour of the IGBT. Three tests were carried out to assess the performance of the IGBTs, namely as operation under different ambient temperatures, different switching frequencies and finally, when operated under different electrical loading. All tests took place simultaneously under same conditions to ensure repeatability and confidence.

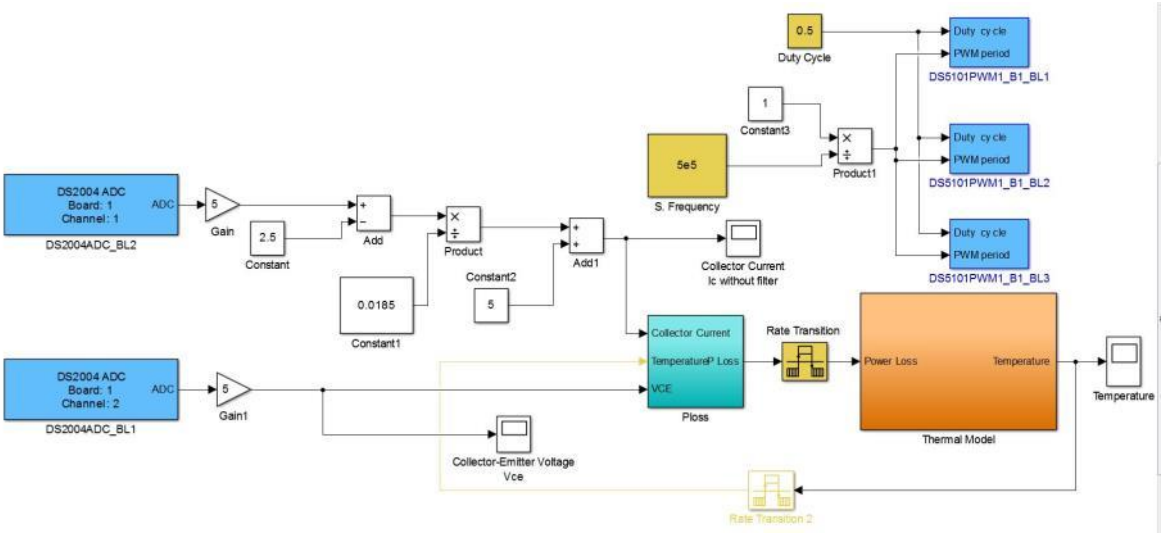


Figure 3.59: Real-time implementation of electro thermal model in DSAPCE

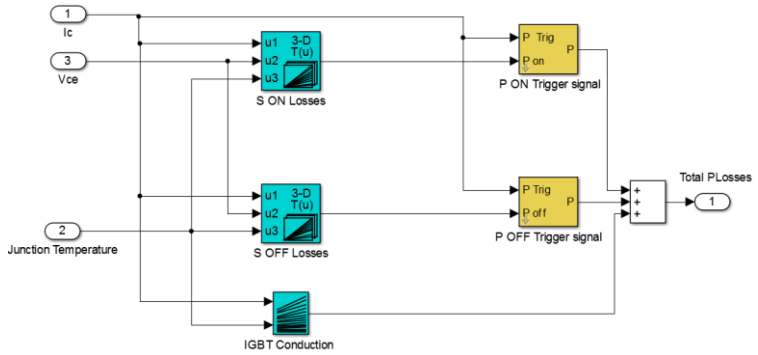


Figure 3.60: View of the power loss block in dSPACE

3.25.1 Ambient Temperature Effect Test

All units were operated under the same conditions and ambient temperature was increased in steps of 5°C up to 50°C starting from room temperature of 25 °C. Junction temperature of each IGBT was accurately identified at each ambient temperature when reached to a steady state by using a thermal imaging camera.

3.25.2 Switching Frequency Effect Test

In the switching frequency test, the devices were simultaneously driven by four sets of different switching frequency from 10-40 kHz. Heat sinks were used in those tests with a collector current of 5A through each switching device.

3.25.3 Load Variation Effect Test

In this test, the devices were examined under different loading conditions. The ambient temperature and switching frequency were kept constant to 30°C and 20 kHz respectively. Loading was varied from zero to full load in steps of 20%. Three sets of boost converter units are shown in Figure 3.61.

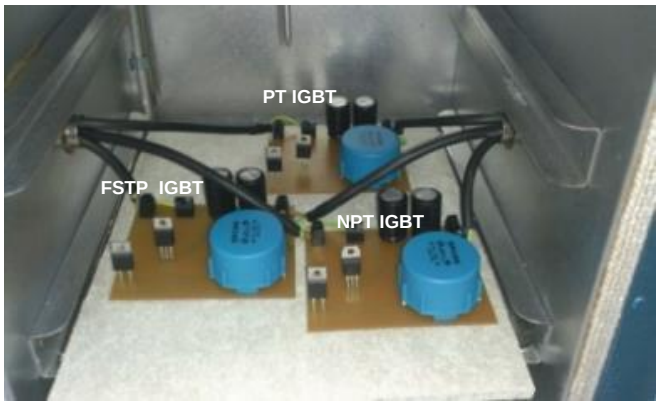


Figure 3.61: Boost converters in temperature controlled chamber

3.25.4 Finite Element Modelling and Numerical Solution

A 3-D finite element IGBT model was derived using COMSOL Multiphysics modelling software. The heat distribution through each material was determined using heat diffusion equation. Material properties such as conductivity and coefficient of thermal expansion are temperature dependent. View of the meshed FE model for TO-220 package and the region for the applied real time power loss profile can be seen in Figure 3.62 (a) & (b), respectively. The collector pin is directly attached to the case. The gate and emitter on the other hand are connected to wire bonds. Chip areas can also be seen in Figure 3.62 (b) for each IGBT technology.

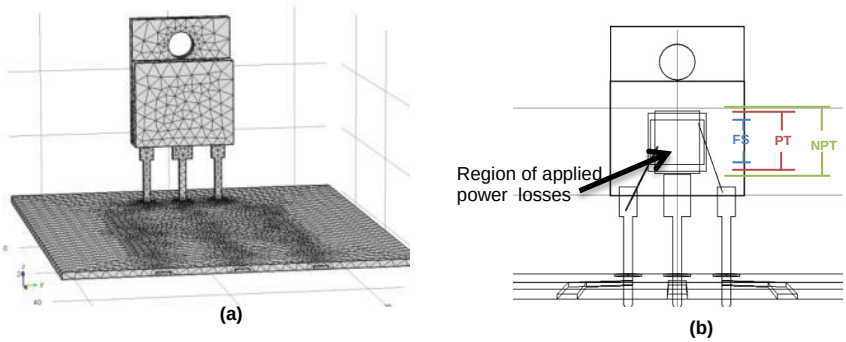


Figure 3.62 (a) View of the FE model and (b) applied heat regions

The heat transfer coefficient *h* is defined as 5 W/m^2K over the model representing natural convection in heating unit. For higher current applications, heat sink model is built in rear side of the case through mica layer where the thermal grease boundary is defined as heat remover boundary condition. Leads are attached by soldering layer on to a PCB via copper channels. Material properties of each layer are listed in Table 3.12.

Table 3.12: Material Properties

Layer	Physical Properties at 25 °C		
	p (kg/m^3)	*k(W/mK)*	*c(J/(kgK)*
Silicon	2330	153	703
Copper	8850	398	380
Gold	19300	318	129
PLCC	900	0.2	1700
Steel Alloy	7850	54	477
Mica	2883	0.71	500
Aluminium	3010	180	741
Grease	-	2	-

3.25.5 Electro Thermal Model of Boost Converter in Simulink

An electro thermal was simulated in Simulink for the boost converter. Collector current and voltage were embedded in previously developed electro thermal models by using energy losses data supplied in manufacturer data and experimentally obtained thermal impedance parameters. The view of the model can be seen in Figure 3.63.

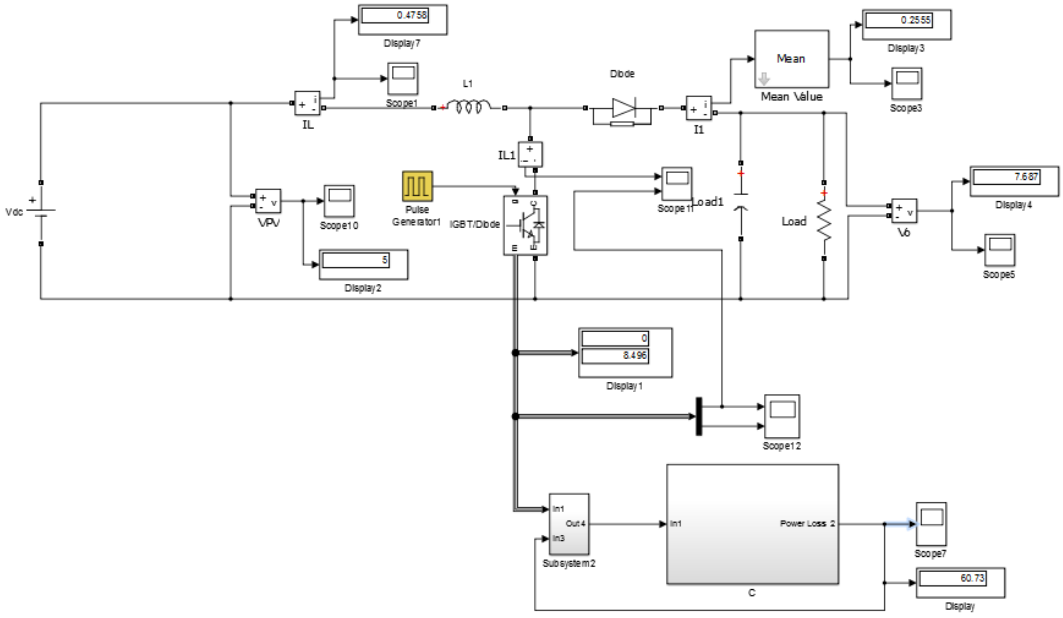


Figure 3.63 View of the boost converter in Simulink

Component parameters were selected as identical with the physically built boost converter. Simulation temperature results used in boost converter can be depicted in Figure 3.64 for each IGBT. As it is shown, NPT showed higher temperature profile compared to the FSTP and PT. PT also showed earlier response to reach for steady state while FS temperature was calculated as 61 °C, approximately 7 °C less than NPTs'.

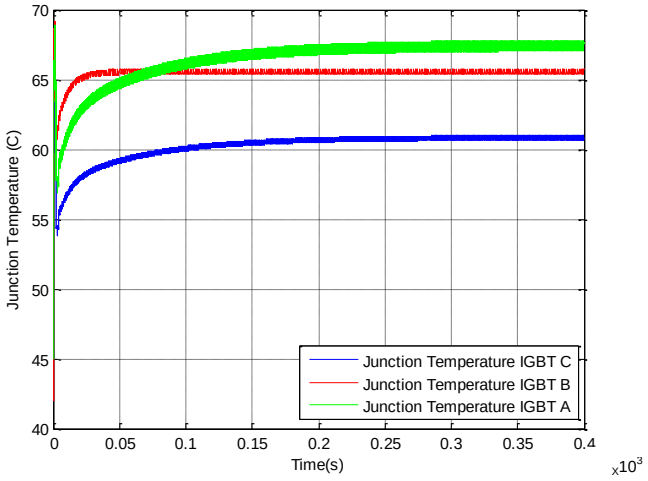


Figure 3.64 Simulation results for each IGBT

3.26 Results and Discussion

3.26.1 Ambient Temperature Influence Test

Supply voltage to each boost converter was 5V with 0.5A of input current at 25 °C ambient temperature. The collector to emitter voltage and current signals are shown in Figure 3.65.

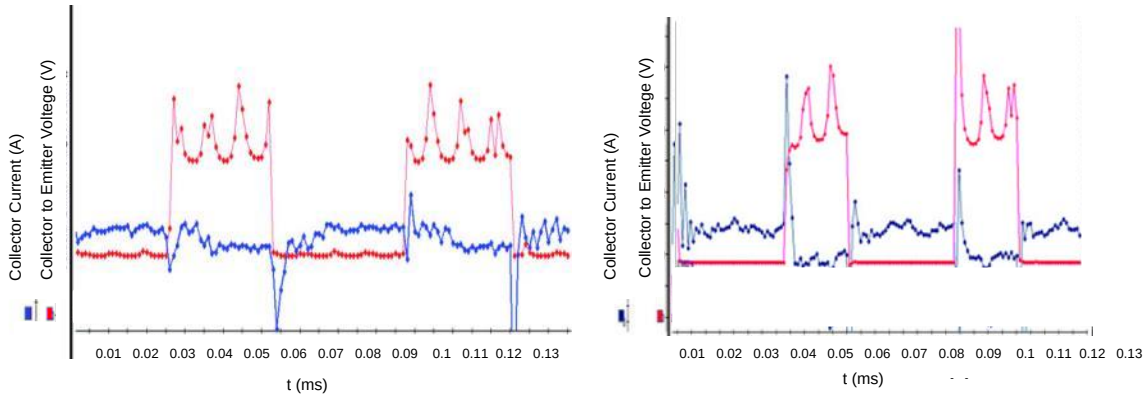
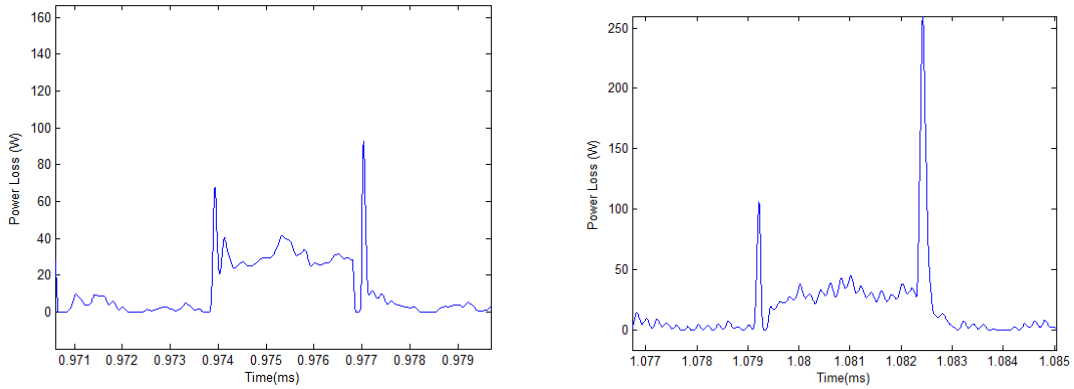


Figure 3.65 Switching transient of (a) NPT (b) FSTP IGBTs

The switching transient is much smoother in the FSTP device due to the additional field stop layer while the NPT showed longer transient in the same period. The effect of the longer tail

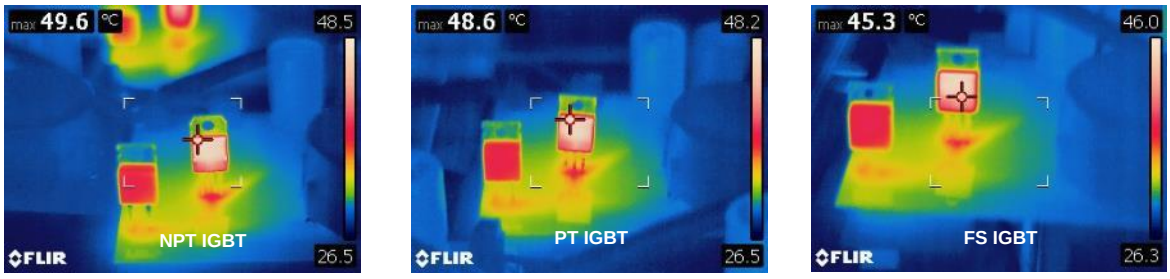
current was also reflected on total power losses where the switches off losses are higher for the NPT, as shown in Figure 3.66.



(a) (b)

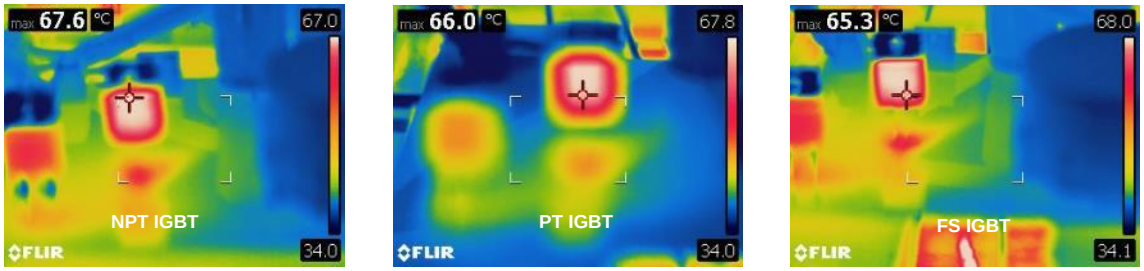
Figure 3.66: View of Power loss profile for (a) FS, (b) NPT

On time losses also increased up to 100 W for NPT where these are only 72 W for FSTP device. Ambient temperature effects on IGBTs thermal behaviour, at 25 and 35°C, are shown in Figures 3.67 and 3.68, respectively.



(a) (b) (c)

Figure 3.67 Thermal camera view (a) NPT, (b) PT, (c) FSTP at 25 °C ambient temperature



(a) (b) (c)

Figure 3.68 Thermal camera view (a) NPT, (b) PT, (c) FSTP at 35 °C ambient temperature

FSTP type exhibits the lowest temperature of 45.3 °C at both tests compared to the PT and NPT, 48.6 °C and 49.6 °C. Power loss was used as inputs to FE model shown in Figure 3.69.

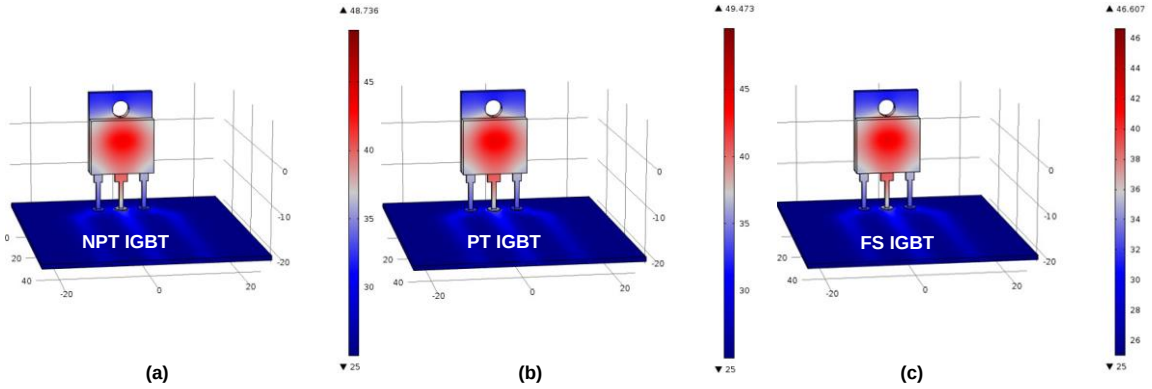


Figure 3.69 FEM of (a) NPT, (b) PT, (c) FSTP at 25 °C ambient temperature

The highest heat was observed around collector lead for all of the IGBTs. The measured temperature for FSTP and PT showed good agreement with the model based calculated figures (~ 1.2°C difference) while the difference was only 0.9°C for the FSTP type. Experimental and model based transient temperature responses for the FSTP device are shown in Figure 3.70 and about ~2°C differences were observed.

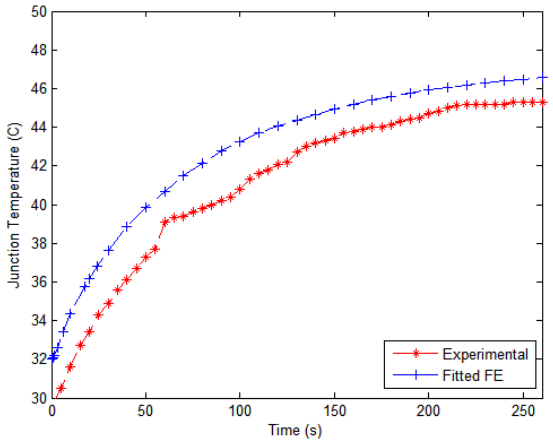


Figure 3.70 Transient temperature in Simulink based experimental dSPACE model and FE model for FSTP

The FSTP type IGBT has shorter drift layer compared to the other two types. Hence, it has lower electric field which punches through the drift region to buffer. This provides shortened tail current and lower power losses. Since the lower losses causes less temperature profile and do not generates experimental peak fluctuations, the error between the experimental and FE based results are observed as low as 1.2 °C.

3.26.2 Influence of Switching Frequency Test

Frequency test results are depicted in Figure 3.71. Device A (NPT) is subjected to highest temperatures at all frequency ranges where device C (FSTP) showed less thermal heating especially at higher switching frequencies.

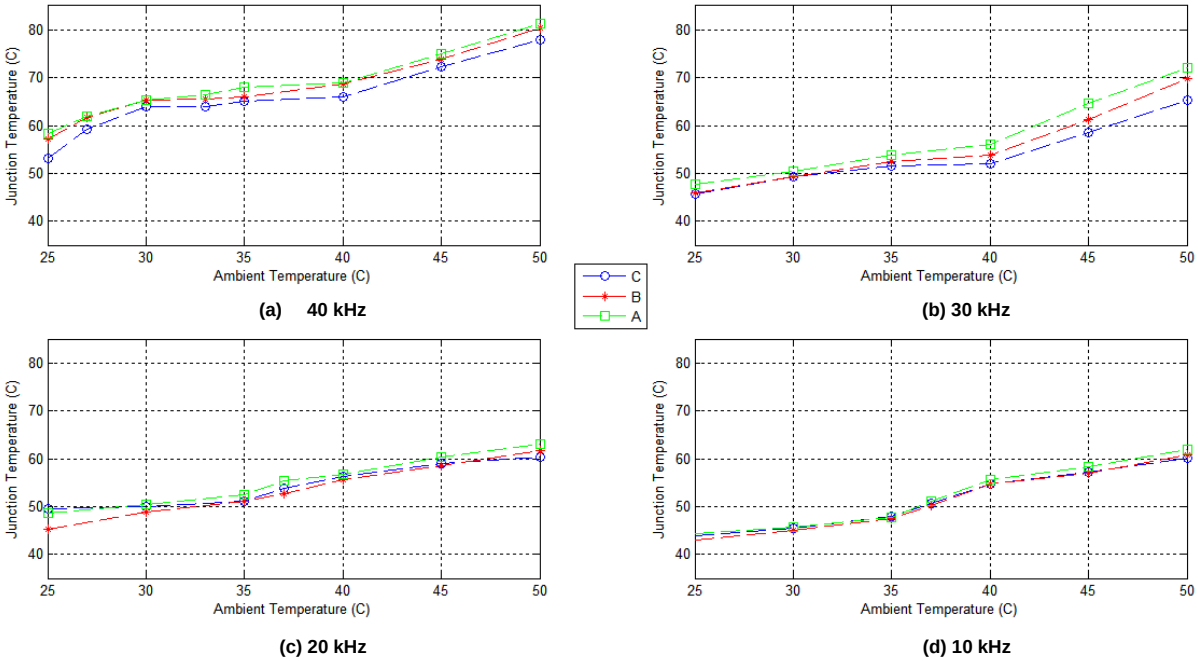
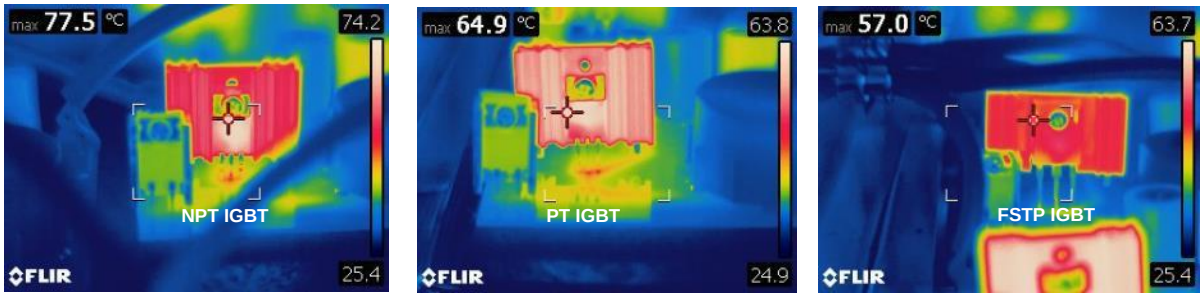


Figure 3.71 Ambient temperature effect on junction temperature at different switching frequencies

Figure 3.72 shows results when the devices were run at 20 kHz switching frequency, 25 °C ambient temperatures and a current of 2 A. The differences in temperature between NPT and FSTP devices were about 20 °C.



(a) (b) (c)

Figure 3.72 (a) NPT (b) PT and (c) FSTP IGBTs at 25 °C ambient temperature with heat sinks attached

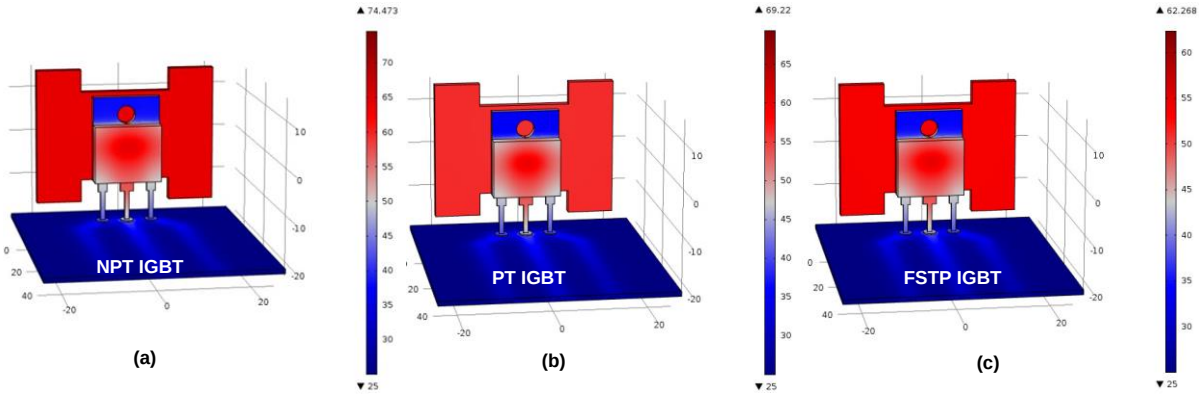


Figure 3.73 FE model of (a) NPT, (b) PT, (c) FSTP at 25 °C ambient temperature with attached heatsinks

Accuracy of model has decreased by approximately 3.7% when higher current was drawn, see Figure 3.73. For NPT, the steady state temperature is 3.2°C lower with FE model, which is 74.4 °C, compared to the 77.6 °C of experimental result. The approximation in physical shape of the heat sink and used thermal grease layer may cause the minor discrepancy. Higher currents may cause change in material properties of the device. Experimental and model based NPT transient temperature responses are shown in Figure 3.74.

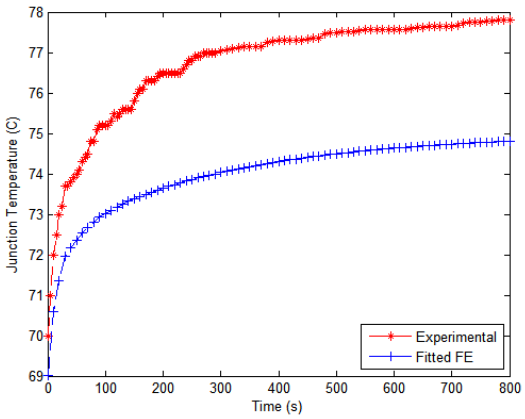
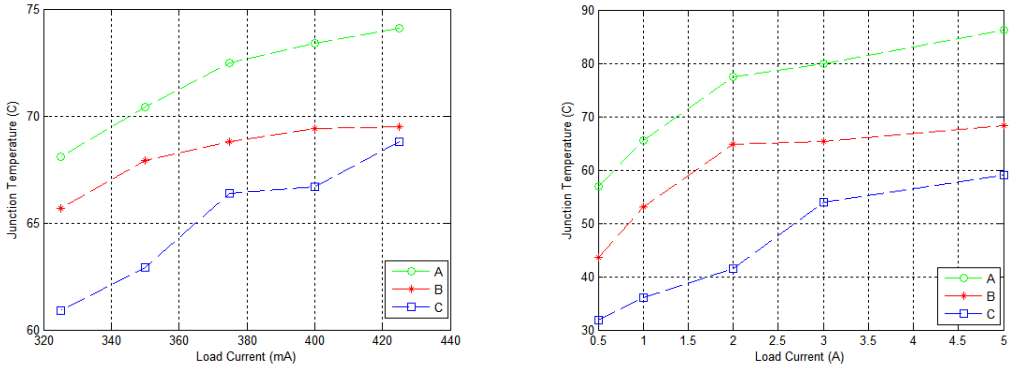


Figure 3.74 Transient temperature in Simulink based experimental dSPACE model and FE model for NPT

The NPT device has the longest drift layer where the electric field dissipates which is different than the other two devices. This increases the tail current and causes higher switching losses. The experimental inaccuracy (3.2°C) is due to the fact that the FE model cannot represent this short time tail current behaviour due to computational time limitations for the NPT device only. The experimental temperature difference was only 1.2 °C for the FS device (Figure 3.70) since it contains very short tail current which becomes almost negligible for the temperature profile. However, it has a considerable effect on the NPT device temperature as advised in [160], [226] and causes temperature estimation errors.

3.26.3 Effects of Load Variation Test

Thermal behaviour of the examined devices due to the load variations is shown in Figure 3.75. As anticipated, the FSTP device was affected much less than the other two devices by load variation. However, it is worth to mention that the temperature changes of the PT device were seen as less dynamic (lowest slope).



(a) (b)

Figure 3.75 Junction temperature at various load characteristics (a) without (b) with heat sink

Efficiency for each boost converter module was also affected by the performance of their switching elements as shown Figure 3.76. The ambient temperature was kept at 30 °C and the operating switching frequency was set to 20 kHz.

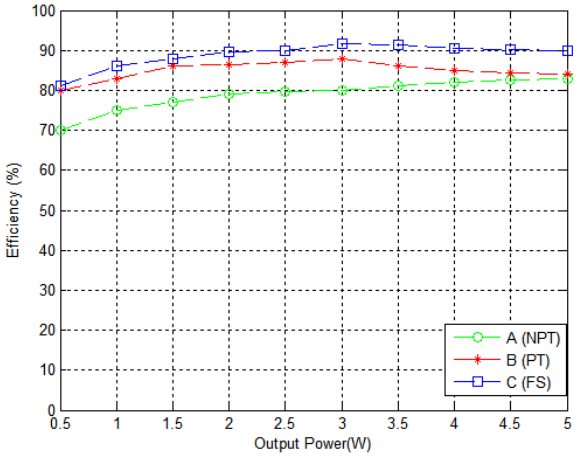


Figure 3.76 Output power efficiency of Boost Converter among each device

The FSTP device was found to be the most efficient one in all of the cases. For example, the FSTP efficiency was about 92 % while it was only 80 % for NPT when the output power was 3W.

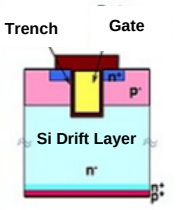
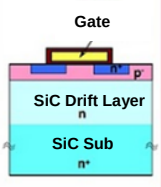
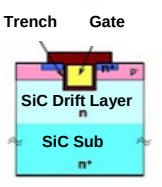
3.26.4 Discussion

Thermal variations are found as not linear and the FSTP device showed consistent behaviour in all cases. PT device had better electro thermal performance compared to NPT. The reason for that is the higher NPT conduction loss as temperature increases due to its positive temperature coefficient. For the FSTP, the presence of field stop layer accelerates the majority carrier recombination during the turn-off intervals and lower saturation voltage drop; hence, its tail current is much smaller than both NPT and PT devices. This leads lower switching losses and temperature characteristics. Regarding to overall performance of modelling approach, about 3 °C temperature difference was observed for FSTP and PT as the current level increased from 0.5 to 2A. Overall, model based predicted results were in good agreement with the empirical data.

3.27 SiC MOSFET Technology compared to Si IGBTs

Conventional IGBTs can be operated at higher current densities with lower frequency while the MOSFETs have better efficiency at higher operating frequencies over 100 kHz**.** In contrast, recently developed SiC MOSFETs have much smaller channel mobility compared to conventional ones [84] which reflect increase in total cost. On the other hand, the thermal conductivity of SiC is much higher than that for silicon [177], so dissipated heat can easily be removed from the device. Regardless of promising material properties of SiC, Si devices can still be more reliable and economically efficient based on the current rating and switching frequency of a specific application. Topological physical differences among Si IGBT and SiC Planar and Trench Gate MOSFETs can be seen in Table 3.13.

Table 3.13: Si IGBT and SiC MOSFET technologies

Material	Silicon	SiC	SiC
Physical Structure			
Technology	IGBT	MOSFET	
Gate	Trench	Planar	Trench

Two trench gate Si IGBTs, namely NPT, which showed weakest thermal performance in previous section, the FSTP, which was the best device in terms of electro thermal performance and a SiC based MOSFET, SCT2280KO by ROHM Semiconductor, specified in Table 3.10 were evaluated. Similar to the previous section, real time power loss data processed through dSPACE Real Time Interface (RTI) and derived as initial heat source in FE models. The experimental test rig is shown in Figure 3.77.

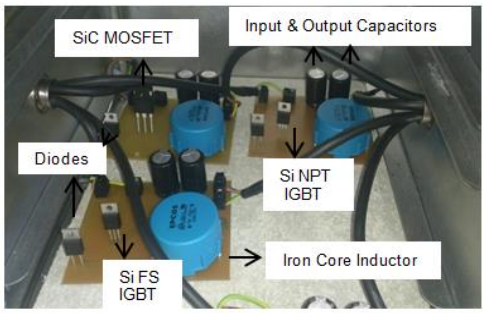
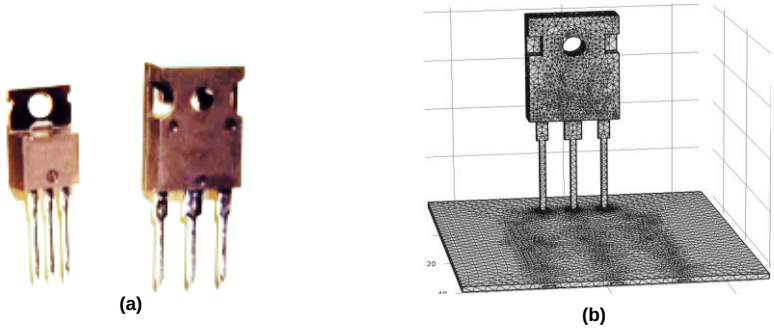


Figure 3.77 Boost converters in temperature controlled chamber

3.27.1 Finite Element Model for SiC MOSFET

Identical modelling approach and boundary conditions were derived from the FE analysis of SiC MOSFET. TO220 package constructed for IGBTs is different than the TO247 for SiC MOSFET in terms of dimension as shown in Figure 3.78 (a). Chip size of MOSFET is almost two times greater compared to both FSTP and NPT IGBTs where FSTP one's is half of NPT's. Mesh view of model can be seen in Figure 3.78 (b). The total number of tetrahedral elements was 57082. Mesh refinement was completed by the scale factor of two especially for the solder layers. Temperature depended material properties for Si and SiC are presented in Table 3.14, and are defined as dynamic arguments where for cooling boundary condition, the natural convection, h, in model was assigned as 5 W/m^2K.



(a) (b)

Figure 3.78 (a) TO-220 (left) and TO-247 (right) Packages, (b) View of FE model for TO-247

Table 3.14 Material Properties Comparison of Si and SiC

Layer	Physical Properties at 25 °C		
	p (kg/m^3)	*k(W/mK)*	*c(J/(kgK)*
T0220 Silicon Chip	2330	153	703
T0247 SiC Chip	3216	490	690

3.27.2 Thermal Measurement and RTI Model Verification

Thermal model was built upon operating switching elements in continuous conduction mode with a constant gate voltage. SiC device temperature had been monitored by thermal imaging and recorded in 5 seconds intervals. Based on obtained transient temperature profile, thermal impedance for each component have been interpolated as in eqns. 3.24 & 3.25 and shown in Table 3.15.

Table 3.15 Thermal impedance characteristics of SiC MOSFET

Device/Parameters	Thermal Capacitances			Thermal Resistances		
	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$
SiC MOSFET	0.51	0.050	0.002	0.153	0.14	0.4003

SiC MOSFET has double thermal capacitance and half of resistance of both FS and NPT IGBTs which is leading to lower thermal fluctuations and amplitude. Figure 3.79 (a) shows thermal images of converters at 25°C ambient temperature when input voltage of boost converter is 5V, switching frequency is 20 kHz and current passes of each device is 0.5A.

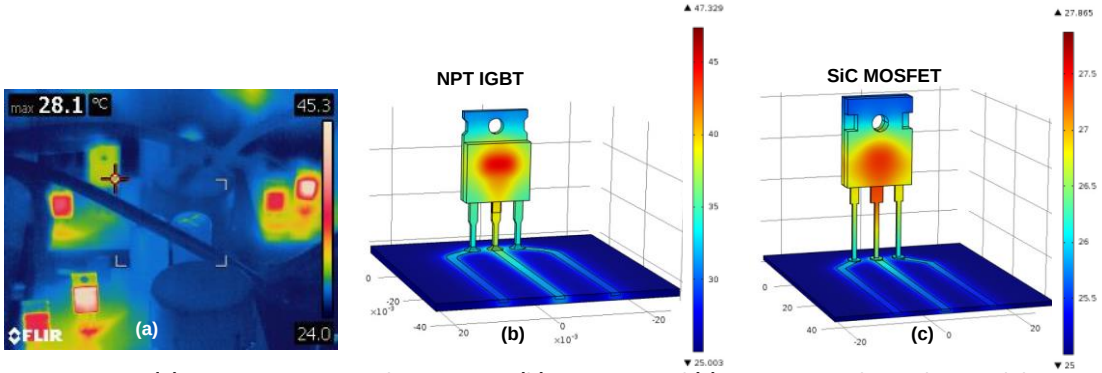


Figure 3.79 (a) Boost Converters in heating unit, (b) NPT IGBT and (c) SiC MOSFET Thermal FE models

FE model solutions of defined devices can be seen in Figure 3.79 (b) for NPT IGBT and Figure 3.79 (c) for MOSFET. Good agreement has been obtained in terms of steady state temperature and total heat distribution over each device. It is distributed through collector

in both results. The NPT IGBT has the highest temperature profile while the SiC MOSFET was subjected to 50% of the NPT's as 45.3 °C and 28.1 °C, respectively.

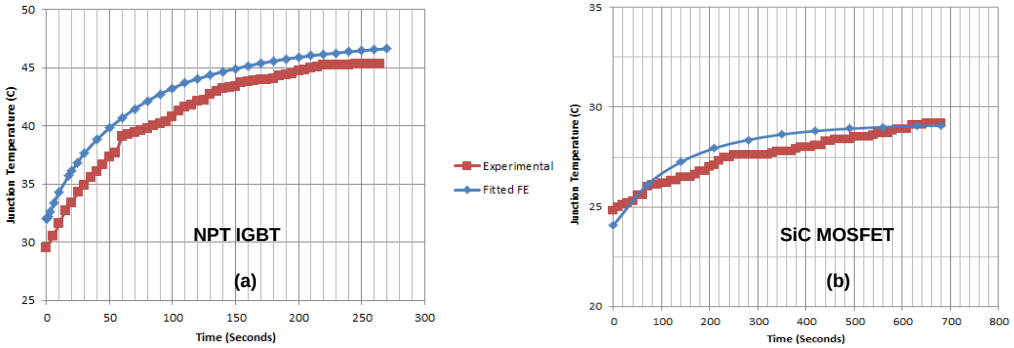
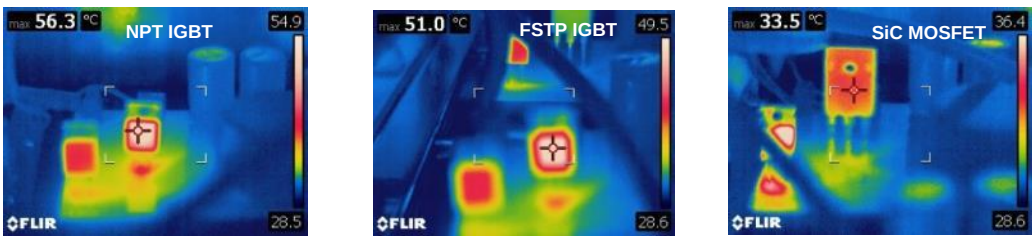


Figure 3.80 Transient temperature comparisons for (a) Si NPT IGBT (b) SiC MOSFET FE models

Approximately 2°C difference was measured for NPT IGBT where this is less than 1°C for MOSFET. Transient temperature results for both devices are shown in Figure 3.80 (a) & (b). It can be clearly seen that the SiC MOSFET has higher heat capacity since it reaches the final temperature around at 800 s whilst this is much shorter for NPT. The accuracy of the proposed FE model approach can still be validated based on transient analysis.

3.27.3 Ambient Temperature and Switching Frequency Effect Tests without Heat Sink

Two sets of experimental tests were performed. First, the devices were operated without heat sinks and, current passes through IGBTs and SiC MOSFET was set as 0.5A by variable resistors. Converters were operated in temperature controlled chamber simultaneously for a set of switching frequencies between 10-150 kHz and the ambient temperature was changed in steps of 5°C from 25 to 50 °C. Temperature of each switching device was monitored by FLIR T440 thermal camera and recorded for each frequency at different ambient temperatures.



(a) (b) (c)

Figure 3.81 Thermal camera view (a) NPT IGBT, (b) FS IGBT, (c) MOSFET at 30°C ambient temperature

Figure 3.81 shows the boost PECs at 35°C ambient temperature when the switching frequency of boost converters was 50 kHz. FSTP IGBT temperature was approximately 5°C less than NPT's while the SiC MOSFET showed better thermal performance compared to both Si IGBT devices with temperature of 33.5 °C.

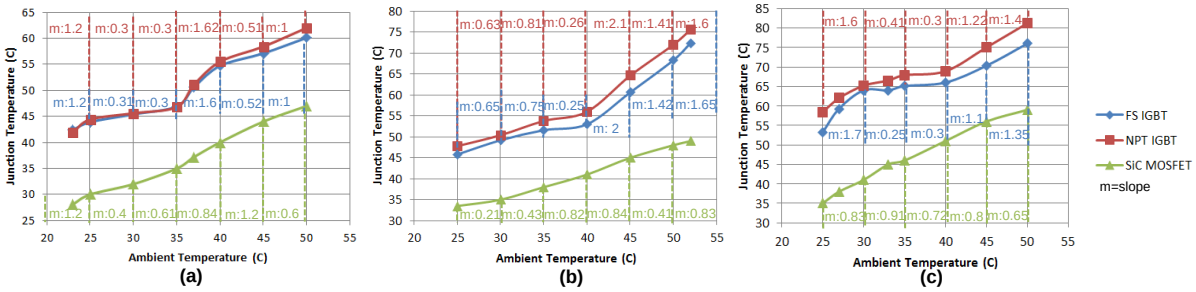


Figure 3.82 Ambient temperature effect on device temperature at (a) 20 kHz, (b) 50 kHz, (c) 150 kHz

For both Si IGBTs, effect of ambient temperature was observed as lower at 35-40°C regions as seen in Figure 3.82. Beyond this point, temperature trend shows higher slope until 55°C ambient. MOSFET temperature showed more linear incline with respect to ambient temperature and can be commented as less ambient dependent especially at higher switching frequencies. Moreover, temperature between both IGBTs increases as frequency inclines due to the higher switching losses of NPT device caused by longer tail current.

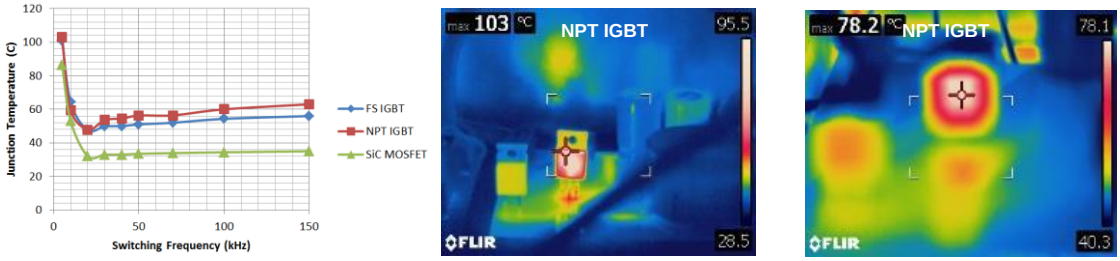


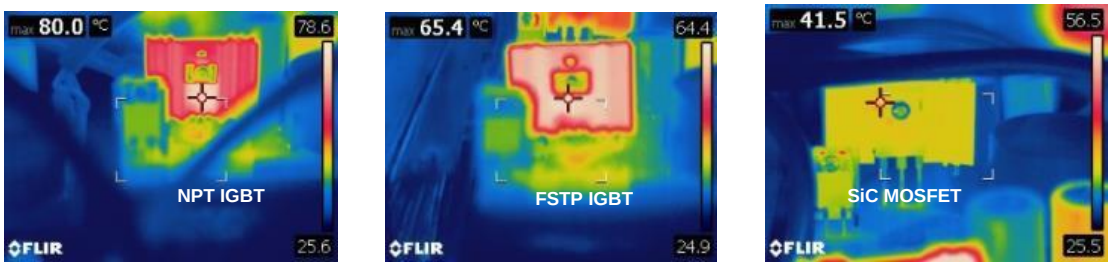
Figure 3.83 (a) Switching Frequency vs. device temperature, (b) NPT IGBT at 103°C and (c) at 78.2°C

The effect of switching frequency is further analysed as shown in Figure 3.83 (a) at 30 °C ambient temperature. The conduction losses are superior at frequencies lower than 15 kHz for each device and hence the temperature rise can be detected up to i.e. 103 °C for NPT as shown in Figure 3.83 (b). Same device has highest temperature of 78.2 °C when operated at 150 kHz at ambient temperature of 40 °C as seen in Figure 3.83 (c). MOSFET is more preferable at higher frequencies as high as 150 kHz. Compared to both IGBTs, its maximum

junction temperature is only increased 2°C while this was 11°C for FSTP and 13°C for NPT IGBTs when the frequency increased from 20 to 150 kHz.

3.27.4 Power Efficiency and Current Effect Operation with Attached Heat Sinks

Further tests have been employed with higher current ratings when heat sinks are attached to the devices. The ambient temperature was kept constant at 25°C and switching frequency of converters was 20 kHz. Boost converters were tested with equal loads, simultaneously.



(a) (b) (c)

Figure 3.84 Thermal camera view (a) NPT IGBT, (b) FSTP IGBT, (c) MOSFET at 25°C ambient temperature

Steady state temperature distributions are shown in Figure 3.84 shows at 2A load current. The temperature difference among each device is approximately as high as 15°C where the NPT has highest temperature of 80 °C and the SiC MOSFET is operated at 41.5 °C. The highest current rating of each device is 15 A and due to laboratory limitation the load current was increased up to 5A. It was found that thermal performance of SiC device decreases as the current rating inclines. The SiC MOSFET is superior Si IGBT devices at higher frequencies. However, Si IGBTs shows more consistent thermal profile at higher current ratings especially above 2A as seen in Figure 3.85 (a). This range can change for different power rating devices. In this study, for accurate comparison, current capacity and total power loss of each device have been selected as same. FE model results for FSTP IGBT and MOSFET can also be seen in Figure 3.85 (b) & (c) when heat sinks are attached at the back of both devices via a thermal grease layer, during high current operation. Processed total power loss data by RTI directly applied to chips in FEM. Good accuracy was also obtained especially for T0-247 packaged MOSFET with only 1.5 °C difference compare to experimental result shown in Figure 3.84 (c).

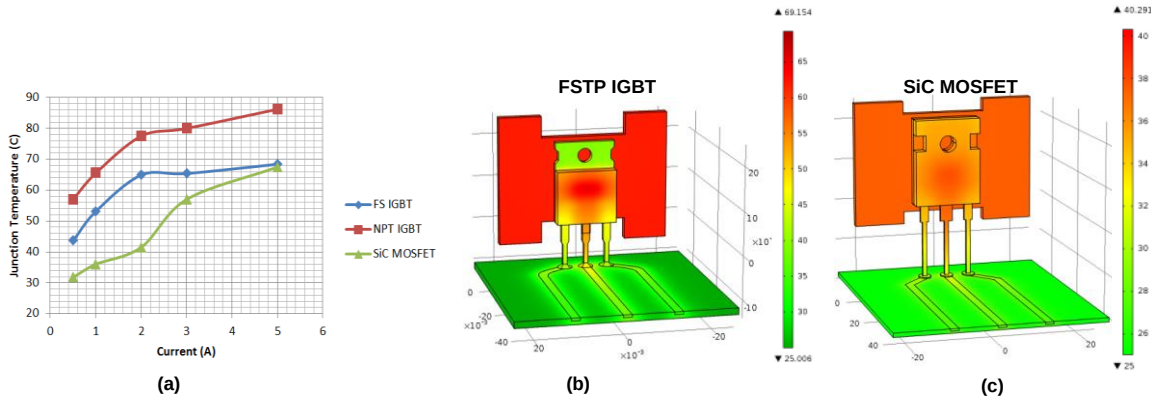


Figure 3.85 (a) Device temperature vs current (b) FSTP IGBT and (c) SiC MOSFET Thermal FE models

For FSTP IGBT, temperature difference is approximately 3.5 °C compared to experimental case due to difference in package type TO-220 and geometrical assumptions on heat sink modelling. As stated before for estimating total power losses and transient temperature, switching transient of each device (on-off state voltage/current) was processed through dSPACE Control Desk into electro thermal models using Simulink are shown in Figure 3.86.

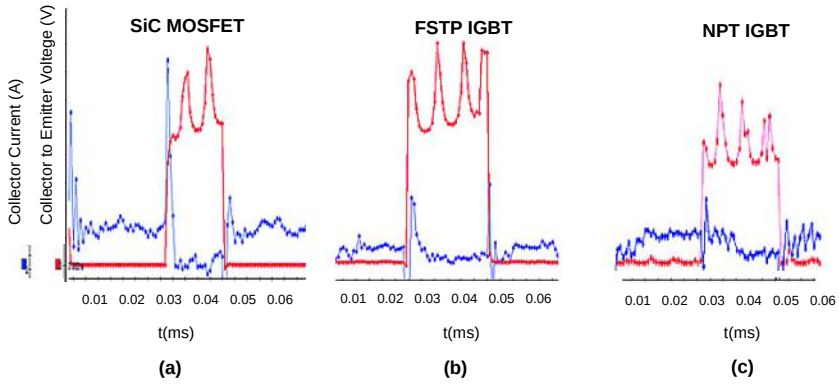


Figure 3.86 Switching transient of (a) SiC MOSFET, (b) FSTP IGBT (c) NPT IGBT

SiC device has very little tail current; hence there is lower switching off losses compared to the both Si IGBTs. This also proves the better thermal performance of MOSFET at higher switching frequencies. On the other hand, NPT IGBT has the highest switching transient time among all devices where the FSTP technology performance is still compatible with SiC MOSFET in terms of thermal performance at higher current ratings. It was also estimated that the conduction losses of NPT's increase as the temperature inclines due to positive temperature coefficient. IGBT costs, evaluated in this paper, are one tenth the cost of SiC MOSFET. As indicated previously, production cost of the SiC device is more expensive. Bigger die size of MOSFET compared to IGBTs, which is three times bigger than NPTs', is also

one reason for expensive device cost. Depending on the priorities of the design, although IGBT companies offer “higher Vce/lower switching energy device” for high frequency applications, and vice versa for a low frequency applications, MOSFET is still effective at the frequencies above 150 kHz in terms of thermal performance. Below this frequency, both IGBTs, evaluated in this study, can be viable competitor of SiC MOSFET especially at higher current limits of an individual device with the help of their lower conduction loss characteristics.

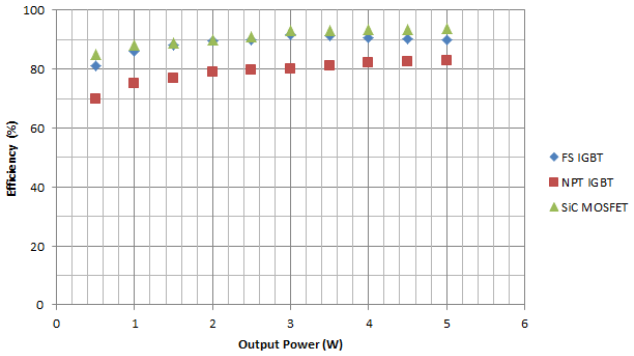


Figure 3.87 Output power efficiency of Boost Converter among each device

Efficiency of boost converter is shown in Figure 3.87 when the ambient temperature was kept constant at 30 °C and the switching frequency was 20 kHz. Under all loading cases, SiC MOSFET based converter was more efficient than the ones with IGBTs. Compared to the NPT IGBT, it attained 10% better efficiency where it is approximately 2% higher once compared with the FSTP device. Efficiency of the FSTP IGBT is very close to the MOSFET performance; however it slightly decreases when the output power is greater than 3.5 W. Table 3.16 shows the temperature comparison for each device while they were operated under 0.5 A load current, 30 °C ambient temperature and 20 kHz of switching frequency.

Table 3.16 Temperature profile comparison for each device with and without heatsink

Device Condition	Without Heatsink	With Heatsink
SiC MOSFET	41.5 °C	32.1 °C
Si FSTP IGBT	68.5 °C	35.4 °C
Si PT IGBT	69.4 °C	44.1 °C
Si NPT IGBT	74.5 °C	58.1 °C

As it can be observed from Table 3.16, with usage of the heat sinks the device temperatures can drastically be decreased. The most temperature reduction was observed as 30°C for the

FSTP type IGBT which has very similar temperature characteristic with the SiC MOSFET with 32.1 °C and 35.4 °C, respectively. The field stop layer of the FSTP device provides fast recovery and this result in an improved temperature profile. On the other hand, approximately 20°C temperature decrement was achieved for both PT and NPT devices.

3.28 Summary

3.28.1 Electro thermal Modelling of Power Electronic Converters

In this chapter, an electro-thermal model for power electronics module DIM1200ASM45 was developed. The commercially available circuit simulators cannot represent the actual heat flux distribution through the device. Therefore, 3D FEM thermal analysis has been developed to estimate heat interactions between different internal layers of the module. Multi-chip design technology brings the disadvantage of highly complex temperature profile. The cross coupling effects occur through the hidden layers that cannot be easily estimated in practice; hence, different than the studies in literature, the proposed model defines each heat path of the individual components. The developed electro thermal model is used to represent the actual thermal behavior of the each chip on the power module in Simulink. The maximum chip temperature was found as 20°C with the proposed study compared to the conventional method results which ignore the cross coupling effect across individual chips. It can be concluded that the proposed method is well-suited for monitoring the internal behavior of the thermal effects within power electronic modules under their working conditions.

3.28.2 Real-Time Electro thermal Modelling of Power Electronic Converters

Powerful and inexpensive system to monitor the real-time electro thermal characteristics of IGBTs used in boost converters was implemented in this chapter. Compared to the expensive thermal imaging techniques in literature, the system determines IGBTs temperatures and heat distributions based on current and voltage measurements and embedded models. Furthermore, real time electro thermal monitoring study was presented

for SiC MOSFET and Si based IGBT devices within DC/DC boost converter. Finite element model of these semiconductor components was developed as a function of power loss real-time measurements. The study demonstrates good agreement between model outcomes and obtained experimental results under different environmental and operational conditions such as ambient temperature and switching frequency. SiC device was found more thermally stable particularly at frequencies higher than 100 kHz and has approximately 20°C less operating temperature characteristic compared to the IGBT devices in most of the tested conditions. FSTP IGBT performed the best at frequencies between 10-50 kHz thanks to its lower conduction loss characteristics. The switching frequency is significant since higher switching frequency decreases the fluctuations and this brings the ability to decrease the size of the output capacitor and inductor to save converter space and cost. However the efficiency is decreased as switching frequency is increased due to the increased switching losses. In conclusion, SiC device has a better dynamic response since it has a wider band gap and can block higher voltage and reduce drift region widths due to its higher electric field. Lower recovery current characteristic is also leading to less switching losses. Other outcome of this chapter is that the Si IGBTs can be selected as switching device for boost converters used in wider frequency range applications if cost matters. The results were verified by comparing the analytical results and further experimental validations. The proposed models will also be extended for providing thermo mechanical thermal stress analysis in Chapter 4 and life consumption monitoring in Chapter 5.

Chapter 4

Thermo Mechanical Modelling of Power Electronic Modules

4.1 Overview

Based on the surveyed research work [183-190], there is still a need for an accurate IGBT model to understand its thermos mechanical characteristics under wide weather condition variations. Thermally induced effects, e.g., thermal stress caused by temperature fluctuations, of the dynamic DC link operation have not been thoroughly analysed in literature [190-195], as well. Therefore, thermo mechanical modelling of power electronic modules was initially derived in this chapter. Then, based on the obtained temperature-thermal stress relation, it offers a new switching frequency driving scheme by considering the DC link voltage requirements. A conventional 1.7 kV/1 kA dual IGBT power module, by Infineon, was used to build power electronic converter (PEC) of a wind energy system in Simulink. The developed scheme was embedded in power loss models to minimise temperature fluctuations. The performance of the proposed scheme was compared with the conventional back-to-back topology based constant and dynamic DC link operations. A finite element model (FEM) combined with a Simulink code was established to monitor PECs thermally induced stress based on estimated power loss profiles for different topologies.

4.2 Thermo Mechanical Modelling of Power Electronic Modules

As stated in [1], the effect of temperature cycling can also be explained by typical stress-strain curve defined as cyclic stress shown in Figure 4.1 where; σ is the cyclic stress, i.e. temperature cycling and ε is the deformation. Operating the device at high temperatures may not cause instant failures; however it produces degradation that leads to eventual breakdown at medium to long term period [16].

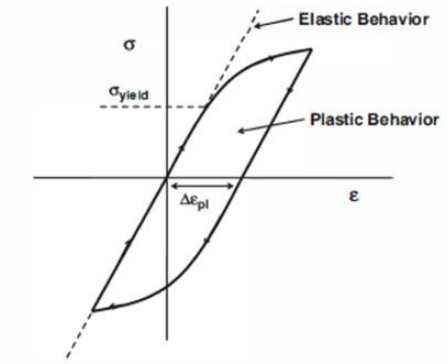


Figure 4.1 Typical stress-strain (σ-ε) curve [11]

With a low cyclic stress below, no damage occurs and the material is in the elastic region. When the stress is increased above this point, deformation begins and the material enters into the plastic region [1]. The mismatch among adjacent layers of the module is non uniform due to the coefficient of thermal expansions (CTE) differences of each material. Especially, the high difference among solder materials ($Pb_{40}Sn_{60}$ or SAC305) and silicon chips and substrates (AlN or Al_2O_3) in terms of CTE causes bimetal effect when the module is subjected to temperature fluctuations [27] [113]. Hence, thermally induced stress occur which causes deformation and eventual cracks based on the stored elastic energy. In order to present stress-strain and maximum stress (von Misses) distribution, the FE model was subjected to the power loss profiles (not constant step input). In the model, the stress distribution was defined by the yield function *F* as:

$$F = \sigma_{mises} - \sigma_{yield} \tag{4.1}$$

where σ_{yield} is the yield stress and σ_{mises} is the von Mises stress. It is derived from the deviatoric stress tensor, which considers the stress due to the shape changes and is given as;

$$\sigma_{mises} = \sqrt{\frac{3}{2} dev(\sigma) \; : \; dev(\sigma)} \tag{4.2}$$

It is used in failure tests [27] where the maximum von Mises stress should be less than the yield strength in such operations. Anand's model [109] was used to describe the solder behaviour such as temperature sensitivity, creep and strain hardening. It is a time-dependent plastic phenomenon which formulates viscoplastic deformations. The constitute model equations are defined firstly by flow equation as:

$$\dot{\varepsilon}_{isr} = A \exp(-Q / RT) \left[\sinh(\xi \frac{\sigma}{s}) \right]^{1/m} \tag{4.3}$$

where $\dot{\varepsilon}_{isr}$ is the effective inelastic strain rate, *A (17.9 1/s)* is the pre-exponential factor, *Q* is the activation energy *(82895 J/mol)*, *R* is the Boltzmann's constant*, T* is the temperature, ξ *(0.35)* is the stress multiplier , σ is the tensile stress and *m (0.153)* represents the strain rate sensitivity of stress. Then, the evolution equation is defined with respect to scalar variable *s* (deformation resistance*)* as:

$$\dot{s} = \left[h_0 (|B|)^a \frac{B}{|B|} \right] \dot{\varepsilon}_{isr} \tag{4.4}$$

where,

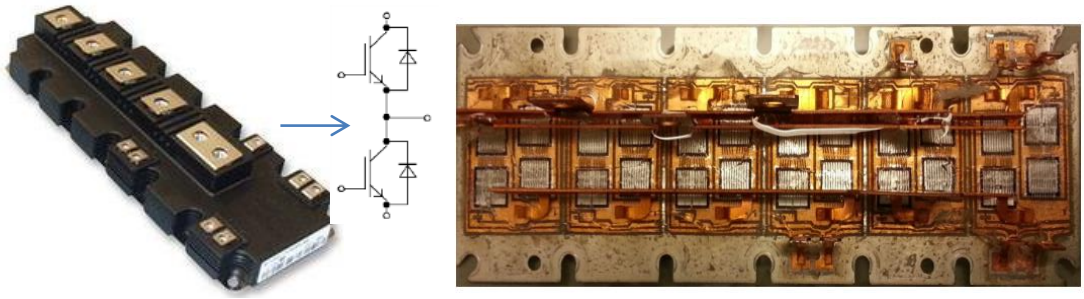
$$B = 1 - s / s^* \tag{4.5}$$

$$s^* = \hat{s} \left[\frac{\dot{\varepsilon}_{isr}}{A} \exp(Q / RT) \right]^n \tag{4.6}$$

h_0 *(1526 MPa)* states the hardening/softening constant, *a (1.69)* is the strain rate sensitivity of hardening/softening, s^* represents the saturation stress, $\hat{s}$ *(2.536MPa)* is the coefficient for saturation, *n (0.028)* is the strain rate sensitivity of deformation resistance [241].

4.3 State of the Art Thermo mechanical Model of IGBT Power Module

As stated earlier, a dual IGBT power module, namely the FF1000R17IE4, by Infineon was purposely selected for this study due to its manufacturing topology which suits well as one phase (leg) in two level back to back scheme of PEC topology [95]. It is also suitable for wind PEC application operated at 1.1 kV DC link voltage with 1.7 kV/1 kA rating. Physical and unmounted views of FF1000R17IE4 are seen in Figure 4.2 (a) & (b), respectively. The device has twelve IGBT and twelve recovery diode chips.



(a) (b)

Figure 4.2 (a) Physical and (b) unmounted view of the FF1000R17IE4

The thermo mechanical FE model was implemented for the selected IGBT module and an attached heat sink was modelled using COMSOL as seen Figure 4.3 (a). Based on the actual dimensions and the material properties stated in Table 4.1, heat distribution through each material was generated using eqn. 3.13. Material properties such as conductivity or

coefficient of thermal expansion are temperature dependent. Therefore, these were defined as dynamic properties and as function of temperature as shown in Figure 4.3 (b), e.g., for silicon layer. Different than the FE model of DIM1200ASM45 derived in Chapter 3, two cylindrical domains, representing liquid cooling elements, are placed across the heat sink, operated at 25 °C. Bottom surface was modelled as convection boundary, where heat transfer coefficient h is found as 4200 W/m2·K using eqn. 4.7:

$$h = R_{th,hs}.A_{hs} \tag{4.7}$$

where A_{hs} is the surface area and $R_{th,hs}$ is the thermal resistance of the heat sink.

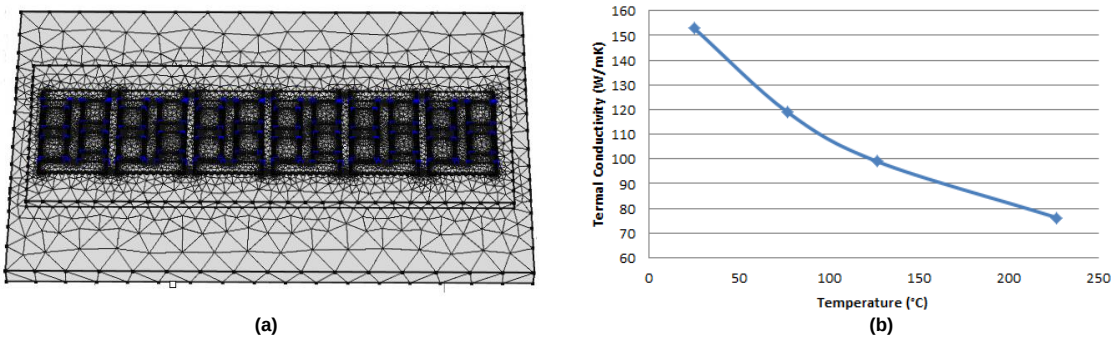


Figure 4.3 (a) Meshed model view of FF1000R17IE4 (b) dynamic thermal conductivity property of silicon layer.

Table 4.1 Physical properties of each layer material at 25 °C [45] [242] [241] [243]

Layer	Physical Properties at 25 °C					
	ρ (kg/m^3)	K (W/m·K)	c (J/(kg·K)	CTE (10^{-6}/K)	Young Modulus (MPa)	Poisson Ratio
Silicon	2330	153	703	3.61	113.000	0.28
Solder	7360	33	200	30.20	27.557	0.40
Copper	8850	398	380	17.30	128.000	0.36
Aluminium	3300	180	750	4.60	344.000	0.22
Copper	8850	398	380	17.30	128.000	0.36
Solder	11,300	35	129	29	16.876	0.44
Baseplate	3010	180	741	0.27	192.000	0.24
T. Grease	2500	2	700	29	15.700	0.32
Heat Sink	2730	155	893	4.30	384.000	0.30

Thermal grease between heat sink and base plate was defined as boundary with 2 W/m·K conductivity. Initially, a constant 200 W heat was applied in time domain on each chip located on the module where the initial temperature was 25 °C. In order to generate

thermal network, simulation was computed until the step response of heating curve reaches steady state as seen in Figure 4.4 (a) & (b).

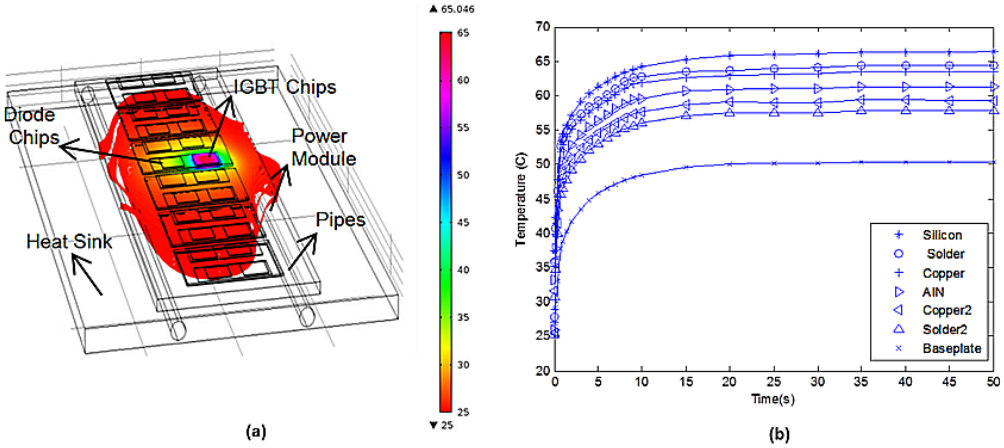


Figure 4.4 (a) Temperature distributions due to heating (b) layer temperature and fitted data

Thermal impedance for each individual layer was extracted by curve fitting using least square method. The thermal matrix, in Laplace domain, was then generated based on the self and coupling heating across [242].

4.4 Thermo Mechanical Modelling of PECs in Wind Energy Systems

PECs, depending on the topology and the application, allow bi-directional power flow [244] between grid and generator side. Two and Three Level converters are two most popular types [245], [95] in wind energy applications. One advantage of the three level converters is that they have additional one more output voltage level ($-V_{DC}/2$, 0, $V_{DC}/2$) compared to the two level topology ($-V_{DC}/2$, $V_{DC}/2$). Output voltages are also smoother with a three-level converter which leads to smaller harmonics but it requires more components and complex control schemes. Two level converters are still preferred in most of the wind applications because of its simpler structure. It is bi-directional power converter consisting of two conventional PWM-VSCs with six unidirectional commanded switch pair (an IGBT and a Diode) used as a rectifier, and with the same number of switch pair, used as an inverter [246]. PEC connection topologies are divided into two categories in wind energy systems; namely, partial scale (PS) and full scale (FS), where doubly fed induction generator (DFIG) is common option for PS topology, as seen in Figure 4.5.

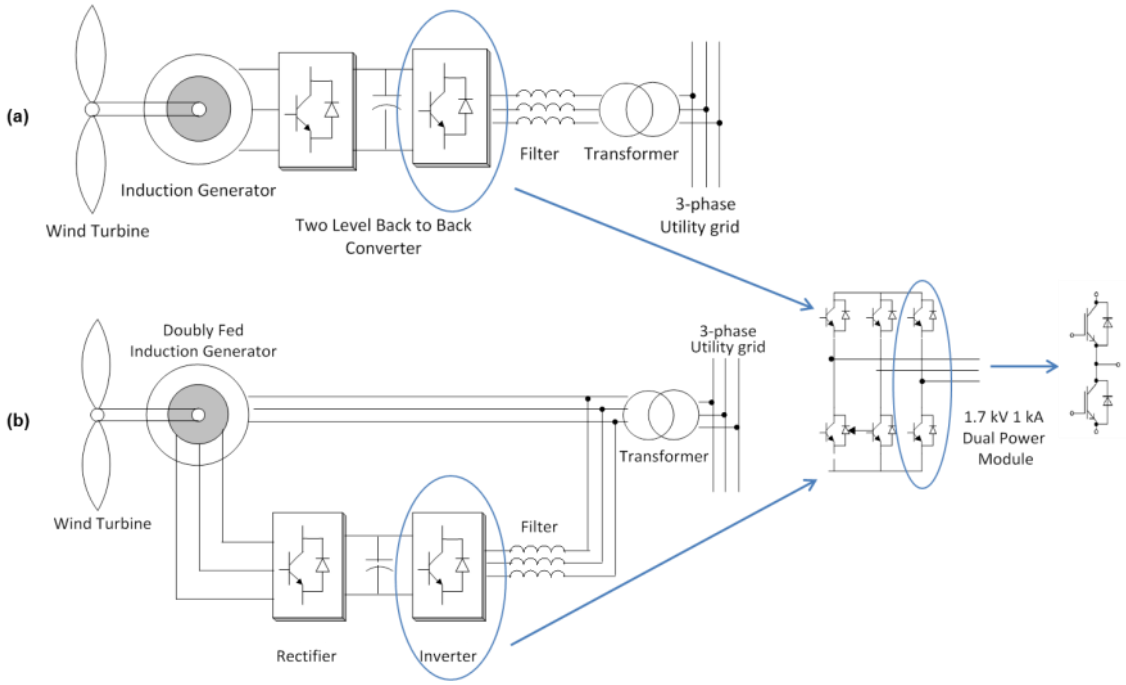


Figure 4.5 Two level back-to-back converter topology in (a) full scale (FS) and (b) partial scale (PS) based wind energy system

Power losses for two level back to back converters are defined based on a sinusoidal output current. As discussed in previous chapters, turn on and off time losses occur in switching transient for IGBTs and recovery losses occur in diodes. Conduction losses, on the other hand, occur in conducting mode of the IGBT and diode chips. Sample sinusoidal power loss signals for an IGBT device, operating in a back to back converter, can be seen in Figure 4.6.

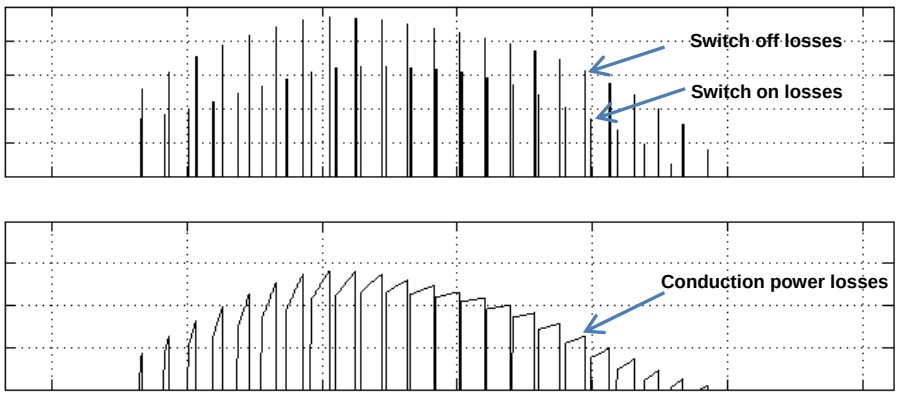


Figure 4.6 Sinusoidal Power losses Signals

As [247] derived, the conduction losses for IGBTs and diodes device operating in a back to back converter can be represented as:

$$P_{CON,IGBT} = \left(\frac{1}{8}+\frac{M}{3\pi}\right)\frac{V_{CE}-V_{CO}}{I_{CN}} I_{CM}^2 + \left(\frac{1}{2\pi}+\frac{M}{8}\cos\theta\right)V_{CO}I_{CM} \quad (4.8)$$

$$P_{CON,DIODE} = \left(\frac{1}{8}-\frac{M}{3\pi}\right)\frac{V_F-V_{FO}}{I_{CN}} I_{CM}^2 + \left(\frac{1}{2\pi}-\frac{M}{8}\cos\theta\right)V_{FO}I_{CM} \quad (4.9)$$

where $P_{CON,IGBT}$ is the IGBT conduction losses, $P_{CON,DIODE}$ is the diode conduction losses, M is the modulation index, V_{CE} is the collector to emitter voltage, V_{CO} is the threshold voltage for IGBT, I_{CN} is the rated collector current, I_{CM} is the maximum collector current, ϑ is the angle between current and the voltage, V_F is the diode forward voltage, V_{FO} is the threshold voltage for diode. Then, switching losses are derived as[247]:

$$P_{SW,ON} = \frac{1}{8}V_{cc}t_{rN}\frac{I_{CM}^2}{I_{CN}}F_S \quad (4.10)$$

$$P_{SW,OFF} = V_{cc}t_{fN}I_{CM}F_S\left(\frac{1}{3\pi}+\frac{1}{24}\frac{I_{CM}}{I_{CN}}\right) \quad (4.11)$$

$$P_{SW,RR} = V_{cc}F_S\left[\left(0.28+\frac{0.38}{\pi}\frac{I_{CM}}{I_{CN}}+0.015\left(\frac{I_{CM}}{I_{CN}}\right)^2\right)\times Q_{rrN}+\left(\frac{0.8}{\pi}+0.05\frac{I_{CM}}{I_{CN}}\right)I_{CM}t_{rrN}\right] \quad (4.12)$$

where $P_{SW,ON}$ is the switching on power losses, $P_{SW,OFF}$ is the switching off power losses, $P_{SW,RR}$ is the reverse recovery power losses, V_{CC} is the DC-link voltage, t_{rN} is the rated rise time, t_{fN} is the rated fall time, F_s is the switching frequency, t_{rrN} is the rated recovery time, Q_{rrN} is the rated recovery charge. Look up tables were used to interpolate the previously defined energy losses as function of device current, saturation voltage and temperature as studied in Chapter 3. Simulink blocks were used to generate thermal impedance equivalence which is integrated within previously defined self and coupling heating based thermal impedances for all IGBT/diode chips and all layers underneath.

4.5 Case Study: Thermo Mechanical Wind Turbine and Utility Grid Modelling

FS and PS based two level back-to-back (BTB) power converter topologies were modelled individually with an induction generator based wind turbine system model in MATLAB/ Simulink. The generator and grid side converters have been modelled separately for both topologies. Then, coupled control was established via DC link according to active power supply. Wind turbine converted mechanical output power is described as:

$$P_m = c_p(\lambda, \beta)\frac{\rho A}{2} v_{wind}\,3 \tag{4.13}$$

where P_m is the mechanical output power, c_p is the performance coefficient of the turbine, ρ is the air density, A is the turbine swept area, v_{wind} is the wind speed, λ is the tip speed ratio of the rotor blade to wind speed and β is the pitch angle where it as taken as zero. The parameters of the wind turbine and generator are given in Table 4.2. The base wind speed of the turbine model is 12 m/s and nominal output power is 1.5 MW. Simulated power characteristic of turbine with respect to speed and output power is seen in Figure 4.7.

Table 4.2 Wind turbine and induction generator parameters

Turbine Parameters	**Value**
Base wind speed	12 [m/s]
Nominal mechanical output power	1.5 [MW]
Max. performance coefficient	0.32
Opt. tip speed ratio	8.1
Generator Parameters	
Nominal power	1.5 [MW]
Rated Shaft Speed	1800 [rpm]
Stator inductance	0.042 [mH]
Rotor inductance	0.08 [mH]
Pairs of poles	2

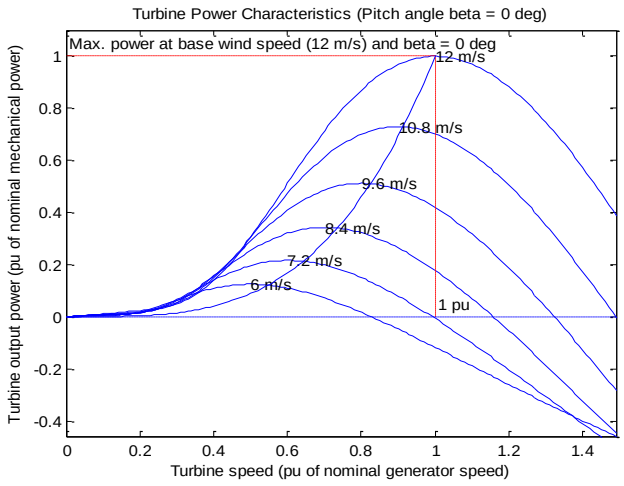


Figure 4.7 Wind turbine characteristics and power-speed curve.

4.5.1 DC Link Voltage Regulation and Grid Side Converter Control

The control for both grid and generator converters was assessed by sinusoidal pulse width modulation method (SPWM). Equivalent voltage equation in a balanced grid connected to a three phase PWM converter through a filter branch is given as [248] [249]:

$$v_L = v_f + v_C \tag{4.14}$$

where converter voltage v_c, filter voltage v_f, line resistance R and inductance L are formed as:

$$v_L = Ri_L + L\frac{di_L}{dt} + v_C \tag{4.15}$$

R can be neglected since it has much lower voltage drop than L and the three-phase voltages ($v_{a,b,c}$) can be represented with respect to line currents ($i_{a,b,c}$) and converter voltages ($v_{ca,b,c}$)as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_{Ca} \\ v_{Cb} \\ v_{Cc} \end{bmatrix} \tag{4.16}$$

The equivalence of eqn. 4.16 in α-β stationary coordinates becomes:

$$\begin{bmatrix} v_{L\alpha} \\ v_{L\beta} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} + \begin{bmatrix} v_{C\alpha} \\ v_{C\beta} \end{bmatrix} \tag{4.17}$$

Then eqn. 4.17 is represented in rotating *d-q* frame as:

$$v_{Ld} = L\frac{di_{Ld}}{dt} - \omega L i_{Lq} + v_{Cd} \tag{4.18}$$

$$v_{Lq} = L\frac{di_{Lq}}{dt} + \omega L i_{Ld} + v_{Cq} \tag{4.19}$$

where ω is the angular frequency. As discussed in, usage of trigonometrical relation leads to define boundary condition by using eqn. 4.18 & 4.19 as [249]:

$$\left| v_{Ldq} - j\omega L i_{Ldq} \right| = \frac{\sqrt{3}}{2} v_{Cdq} \tag{4.20}$$

Assuming $v_{Cdq} = \frac{2}{3} V_{dc}$, $V_{Ldq} = E_m$, where E_m is voltage amplitude, when only active power is supplied to the grid which leads $i_{Ldq} = i_{Ld}$, minimum DC-Link voltage boundary is defined as:

$$v_{dclink} > \sqrt{3E_m^2 + (\omega L i_{Ld})^2} \tag{4.21}$$

Based on the minimum DC-link voltage, PWM signals are synchronised with the grid voltage by zero detection scheme. I_q represents the reactive power component and hence, it is desirable to be zero. Whereas, the desired magnitude for I_d, depends on actual voltage measured across the DC link. The converter output voltages V_{cd} and V_{cq} were regulated based on the difference between measured and reference values of the *d-q* current. Hence, magnitude and phase angle delay of converter output voltages corresponding to grid voltages are set by:

$$v_{L(pk)} = \sqrt{V_{cd}^2 + V_{cq}^2} \tag{4.22}$$

$$\theta = \tan^{-1} \frac{V_{cq}}{V_{cd}} \tag{4.23}$$

4.5.2 Generator Side Control with Switching Frequency Regulation

Similar to the derived *d-q* elements for the three phase line voltages in previous section, stator voltages $v_{sd,q}$ can be expressed as follows [248] [249]:

$$v_{sd} = R_s i_{sd} + \frac{d}{dt} \lambda_{sd} - w_d \lambda_{sq} \tag{4.24}$$

$$v_{sq} = R_s i_{sq} - \frac{d}{dt} \lambda_{sq} + w_d \lambda_{sd} \tag{4.25}$$

where ω_d is instantaneous speed of *d-q* winding set in the air gap, $\lambda_{sd,q}$ and $\lambda_{rd,q}$ are stator and rotor flux linkage expressions, respectively. $v_{rd,q}$ rotor winding voltages are given as:

$$v_{rd} = R_r i_{rd} + \frac{d}{dt} \lambda_{rd} - w_{dA} \lambda_{rq} \tag{4.26}$$

$$v_{rq} = R_r i_{rq} + \frac{d}{dt}\lambda_{rq} + w_{dA}\lambda_{rd} \tag{4.27}$$

where ω_{dA} is the instantaneous speed of the *d-q* winding set in the air gap with respect to the rotor *A*-axis speed. The relation between inductances can be defined as a unit less term leakage factor, σ as:

$$\sigma = 1 - \frac{L_m{}^2}{L_s L_r} \tag{4.28}$$

where L_s and L_r are the stator and rotor inductances and L_m is the magnetization inductance. Hence, the stator windings are defined as:

$$\lambda_{sd} = \sigma L_s i_{sd} + \frac{L_m}{L_r}\lambda_{rd} \tag{4.29}$$

$$\lambda_{sq} = \sigma L_s i_{sq}$$

(4.30)

Then, stator *d-q* voltages can be expressed in terms of control and compensation terms as:

$$v_{sd} = \underbrace{R_s i_{sd} + \sigma L_s \frac{d}{dt} i_{sd}}_{v_{sd}'} + \underbrace{\frac{L_m}{L_r}\frac{d}{dt}\lambda_{rd} - w_d \sigma L_s i_{sq}}_{v_{sd,comp}} \tag{4.31}$$

$$v_{sq} = \underbrace{R_s i_{sq} + \sigma L_s \frac{d}{dt} i_{sq}}_{v_{sq}'} + \underbrace{w_d \frac{L_m}{L_r}\lambda_{rd} + w_d \sigma L_s i_{sd}}_{v_{sq,comp}} \tag{4.32}$$

For the DFIG based partial scale PE control, eqns. 4.31 & 4.32 are derived by eqns. 4.26 & 4.27 for rotor voltages control. The *d-q* voltages can be used to derive equivalent stator generator voltage as:

$$v_s = \sqrt{\frac{3}{2}(v_{sd}{}^2 + v_{sq}{}^2)} \tag{4.33}$$

In steady state balanced conditions, it is equal to the line voltage, V_L, which can be defined in terms of DC link voltage as:

$$v_{L(rms)} = V_{dclink} \frac{\sqrt{3}}{2\sqrt{2}} \tag{4.34}$$

Then, V_{dclink} in eqn. 4.34 was defined as minimum value based on the generator voltage with respect to generator speed. The boundary has been rearranged as:

$$V_{dclink}(\min) > \frac{2\sqrt{2}}{\sqrt{3}} v_{LL(rms)} + \Delta V \tag{4.35}$$

where a control margin is set to ΔV = 10 V. Converter control for both FS and PS topologies can be seen in Figure 4.8.

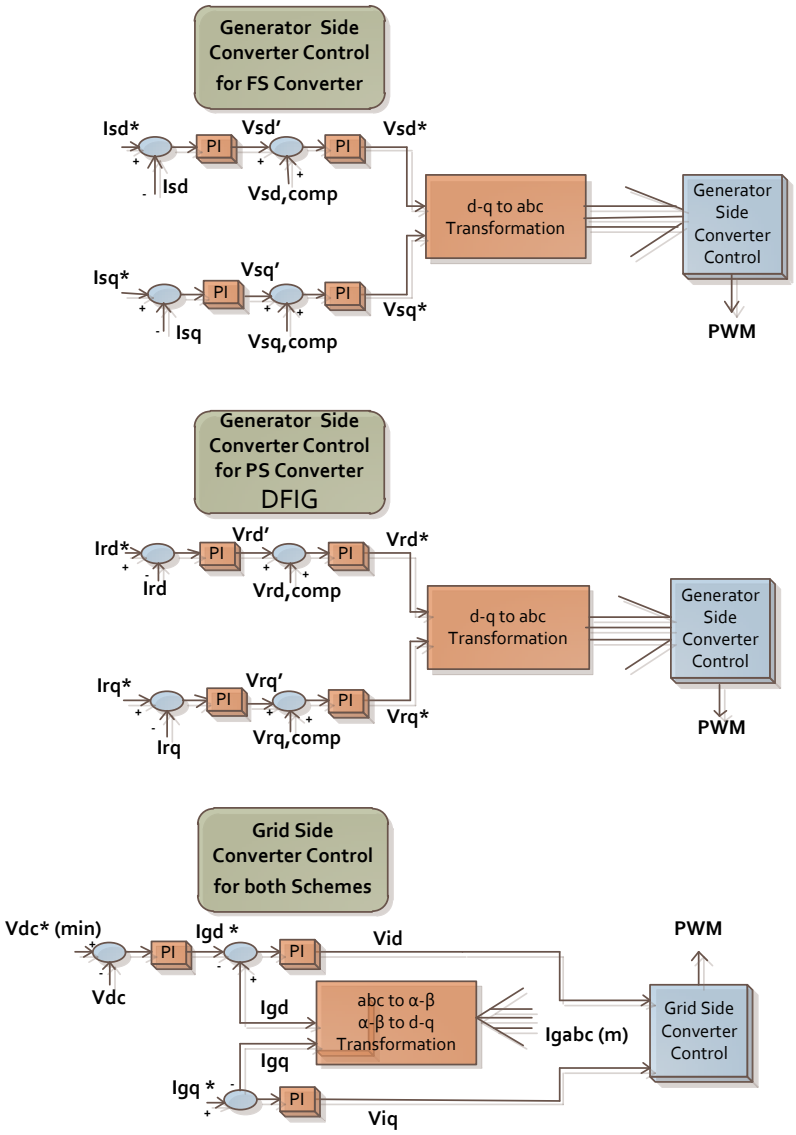


Figure 4.8 View of the control methods of grid and converter side back-to-back converters

Look up tables are used to provide the mechanical torque with respect to reference speed. The mechanical power is also interpolated based on the power *vs.* speed characteristic derived in Figure 4.9. Reference stator *d-q* currents as well as the compensation elements of the stator voltages are also extracted through LUTs data obtained through eqns. 4.29-4.32 by means of angular speed and power. The DC link voltage is adjusted to its minimum value in the DC link calculation block by LUTs during operation. It is derived based on the stored generator voltage and speed data obtained thorough eqns. 4.34 & eqns. 4.35 for the generator side; and based on the grid voltage, active power component I_d and power factor data obtained thorough eqns. 4.20 & 4.21 for the utility grid side. It is then assigned by a scheme according to interpolated value through both sides of PEC. The scheme of the proposed switching frequency adaption is shown in Figure 4.9. In the grid side inverter, the process needs to be monitored in terms of current injection, to protect the switching elements against high power losses. When wind speed decreases and minimum DC link voltage regulation begins, the edge detector block stores the latest calculated power loss for both sides of the PEC. Then, switching frequency regulation block is activated in order to reduce the switching losses. The switching frequency is decreased as the stored power loss is less than the one extracted from active power loss block. When wind speed increases, switching frequency is adjusted according to loss characteristic, as well. The lowest possible operating switching frequency is 2 kHz to mitigate lifetime consumption within converters caused by power cycling load of switching frequency. In order to keep each three-phase voltages in symmetric, switching frequency is adjusted by the ratio of modulation and carrier frequencies (f_m & f_c) in multiple of three as stated in eqn. 4.36.

$$\frac{f_c}{f_m} = 3k, (k \varepsilon N) \tag{4.36}$$

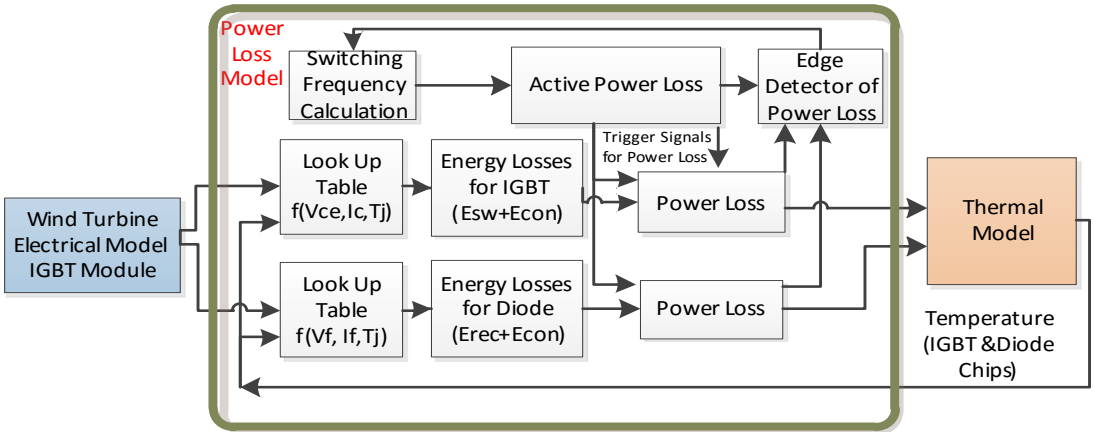


Figure 4.9 Scheme of the electro thermal model with switching frequency adaption

4.6 Results and Discussion

4.6.1 Dynamic DC Link Voltage and Switching Frequency Analysis

The overall modules IGBT on time energy and conduction power losses are seen in Figure 4.10 (a) & (b), respectively. On time energy, losses were expressed with respect to DC current and voltage at generator side converter (GSC) for different wind speeds, as shown in Figure 4.11. When wind speed is lower than the rated wind turbine speed, energy losses can be decreased by lowering the DC link voltage. For instance, approximately 180 mJ loss deduction can be witnessed by reducing the DC link 50%, whilst keeping the current unchanged, when the wind speed is decreased from 12 m/s to 9 m/s.

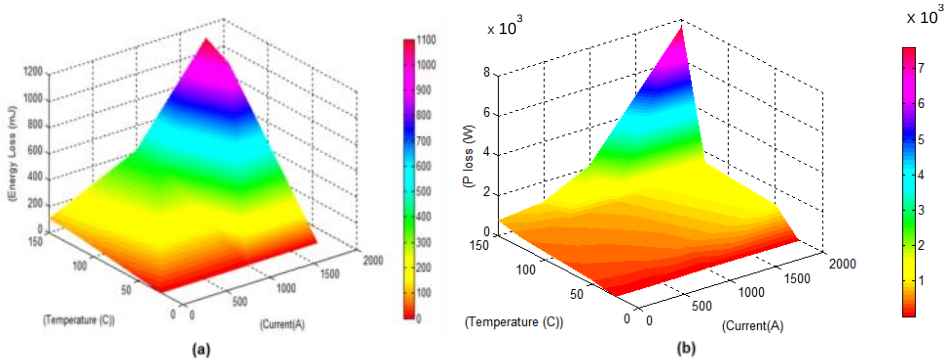


Figure 4.10 (a) Insulated gate bipolar transistor (IGBT) switching-on energy losses; (b) Conduction losses

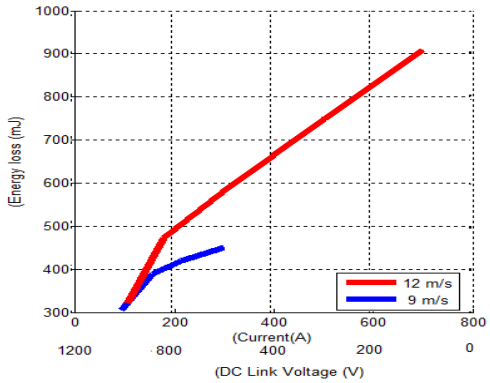


Figure 4.11 DC link voltage *vs.* current *vs.* on time losses

Temperature fluctuations for the GSC with respect to current and switching frequency are shown in Figure 4.12 when the wind speed is 9 m/s. It can be seen that the temperature fluctuations can be kept constant by lowering the switching frequency around 50%, and in the case, current increases approximately 25%.

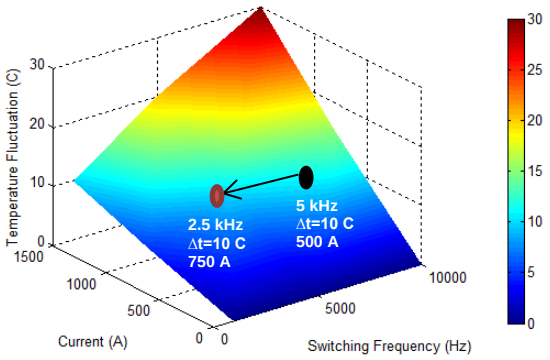
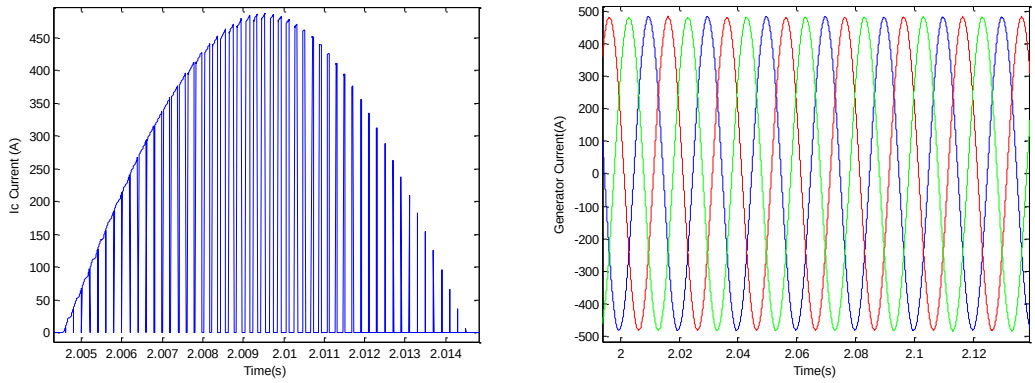


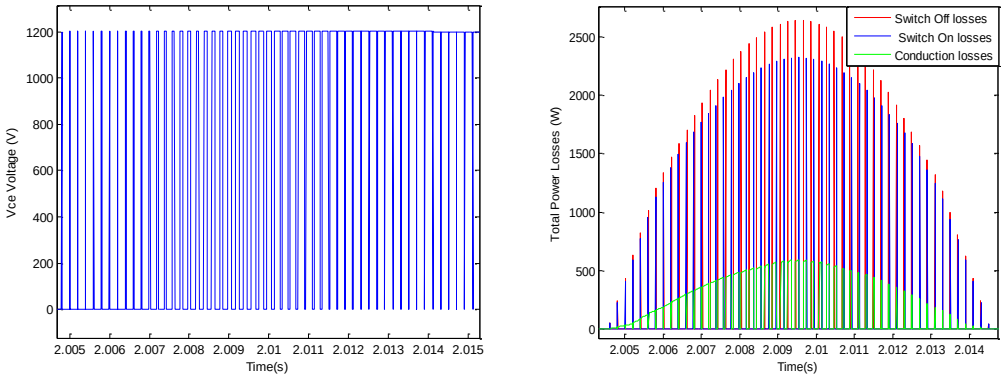
Figure 4.12 Switching frequency effect during 9 m/s wind speed

A sample of collector current profile over a switching period is shown in Figure 4.13 (a), with respect to the grid side converter current of the FS based wind system at 50 Hz, shown in Figure 4.13 (b). The wind speed was kept constant as 12 m/s and the DC link voltage was adjusted as 1.2 kV; hence, the collector-emitter voltage through power devices, appearing at the same level, is seen in Figure 4.14 (a). The switching frequency is 5 kHz. Instantaneous on and off power losses are found as 2.3 and 2.6 kW, respectively as seen in Figure 4.14 (b).



(a) (b)

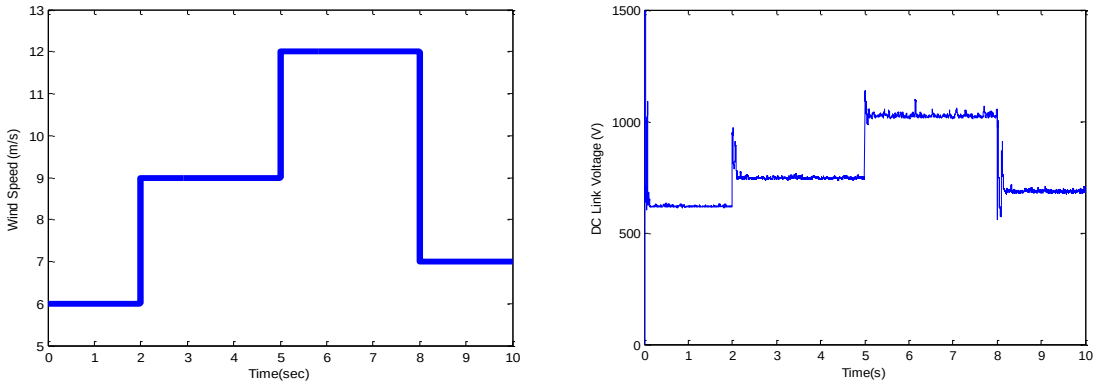
Figure 4.13 (a) Ic current and (b) Three phase generator current



(a) (b)

Figure 4.14 (a) V_{ce} voltage (b) Total power losses at 5kHz

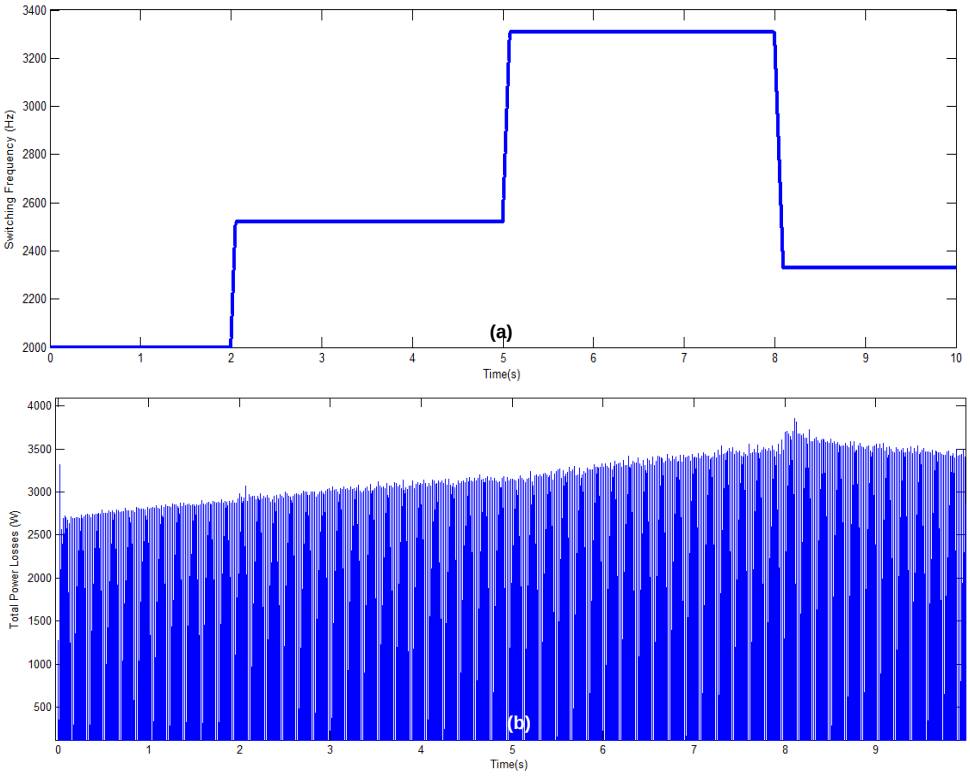
A case study is discussed for FS topology for expanding the switching frequency control. Figure 4.15 (a) & (b) shows a sample applied wind speed profile and the dynamic DC link operation for FS scheme grid side converter, respectively. The initial frequency is selected as 2 kHz where the DC link voltage is 650 V in the model.



(a) (b)

Figure 4.15 (a) Wind speed profile and (b) Adjusted DC link voltage

At *t* = 2 s, wind speed is increased from 9 m/s to 12 m/s. The look up table which obtains minimum value for DC link operation is triggered and increases it to 748 V. At the meantime, the switching frequency is adjusted by the control block shown in Figure 4.9, in order to control switching loss for the assigned current and voltage through the power modules. It holds the latest calculated switching losses before the wind change detected by an edge detector and based on the next calculated power loss signal, the frequency is increased up to 2.55 kHz, as shown in Figure 4.16 (a). Similar operation also takes place at time *t* = 5 s and afterwards until *t* = 8 s. However, at *t* = 8 s, a rapid power loss increase occurs due to higher current injection and frequency controller pulls switching frequency back by means of the ratio defined in eqn. 4.36. The total power losses can also be seen in Figure 4.16 (b) as the DC link voltage is controlled Variable DC link and frequency operation causes fluctuation on the energy supplied to the utility grid. The three phase grid voltage can be seen in Figure 4.16 (c) with distortion caused by the controller. Total harmonic distortion can also be depicted in Figure 4.16 (d) with respect to wind changes and switching frequency adjustments.



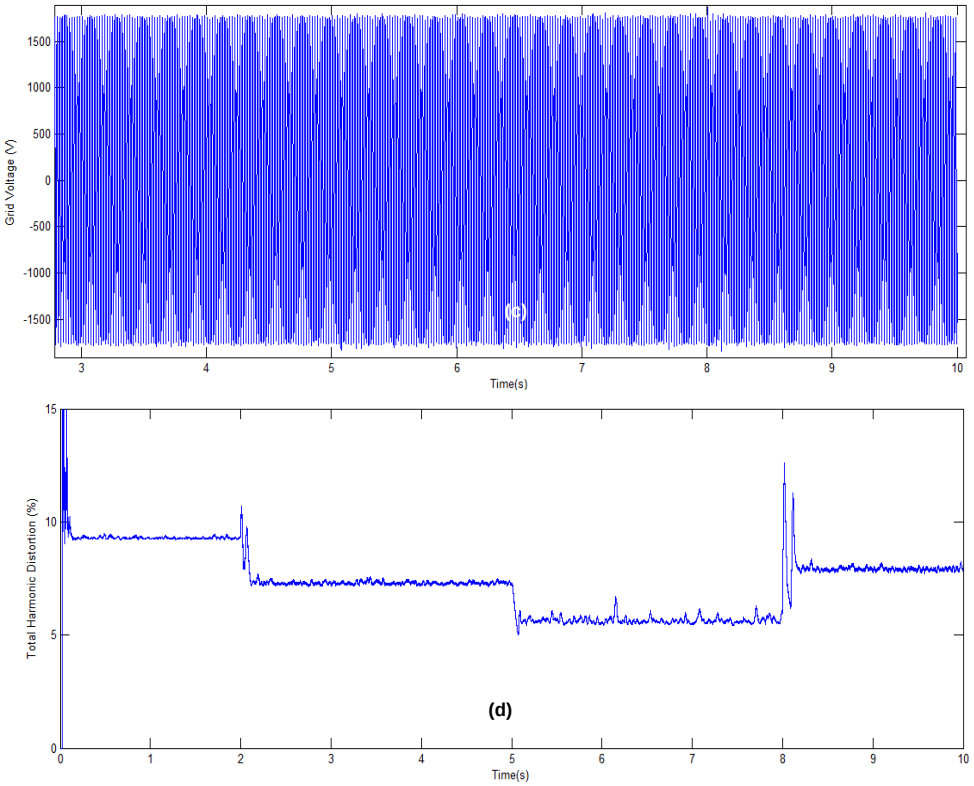


Figure 4.16 (a) Controlled power loss data by dynamic DC link and frequency operation; (b) Power losses; (c) Three phase grid voltage; (d) Total harmonic distortion.

4.6.2 Comparison of Temperature Profiles for FS and PS Based Back to Back PECs

A variable wind profile, shown in Figure 4.17, is applied both PS and FS models for determining the average junction temperature of IGBT chips. The simulation step time was 5 µs. Thermal parameters for the central silicon chip and the layers underneath are shown in Table 4.3 which is obtained through FEM. In order to increase the accuracy, thermal impedances of each extracted curves were represented by three exponential terms. Thermal impedance for thermal grease layer is integrated within baseplate parameters since this layer was defined as a boundary for computational efficiency.

Table 4.3 Thermal parameters extracted from the finite element model (FEM)

Layer	Thermal Capacitance			Thermal Resistance		
	$C_{th,1}$	$C_{th,2}$	$C_{th,3}$	$R_{th,1}$	$R_{th,2}$	$R_{th,3}$
Silicon	0.48	113.14	13.78	0.217	0.056	0.061
Solder	0.69	113.31	13.92	0.212	0.055	0.058
Copper	0.85	113.62	14.22	0.198	0.054	0.057
AIN	1.02	113.94	14.88	0.175	0.053	0.056
Copper	1.57	114.31	15.31	0.154	0.053	0.056
Solder	2.01	114.78	16.04	0.136	0.052	0.052
Baseplate	6.63	115.02	430.0	0.132	0.050	0.009

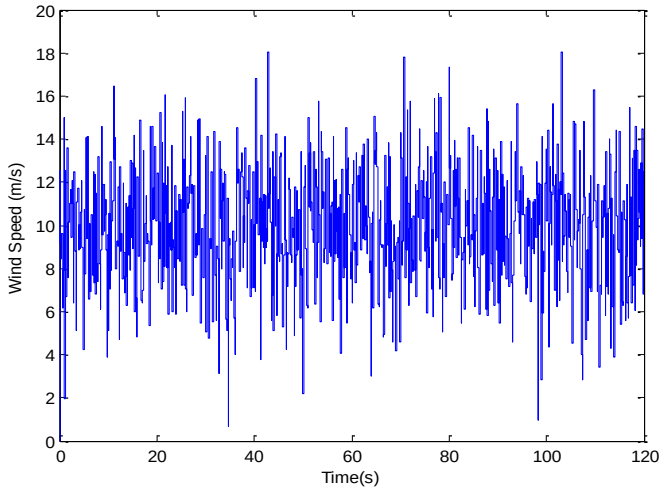


Figure 4.17 Applied wind speed profile

Temperature distributions for GSC and utility grid side (UGS) power modules in FS and PS based wind systems, in three different operation modes, are shown in Figures 12 and 13 respectively. As it is seen in Figure 4.18 (a), temperature distribution with a fixed DC link voltage (1.1 kV at 2.5 kHz) is much stable compared to the variable DC link operation (fixed at 2.5 kHz), shown in Figure 4.18 (b). Especially, at wind speed below the rated shaft speed, the temperature fluctuation is higher. During static DC link operation, mean junction temperature is 92 °C where it is 80 °C for variable DC link operation. On the other hand, the junction temperature profile of the power module, when the proposed control scheme is applied (see Figure 4.18 c), has less fluctuations compared to variable DC link operation. Lower mean junction temperature than with the one with static DC link voltage operation is also attained. It can also be seen that at lower wind speed (at t = 40 s), the temperature is higher compared to the dynamic DC link operation. This is due to the switching frequency increase controlled by the edge detector.

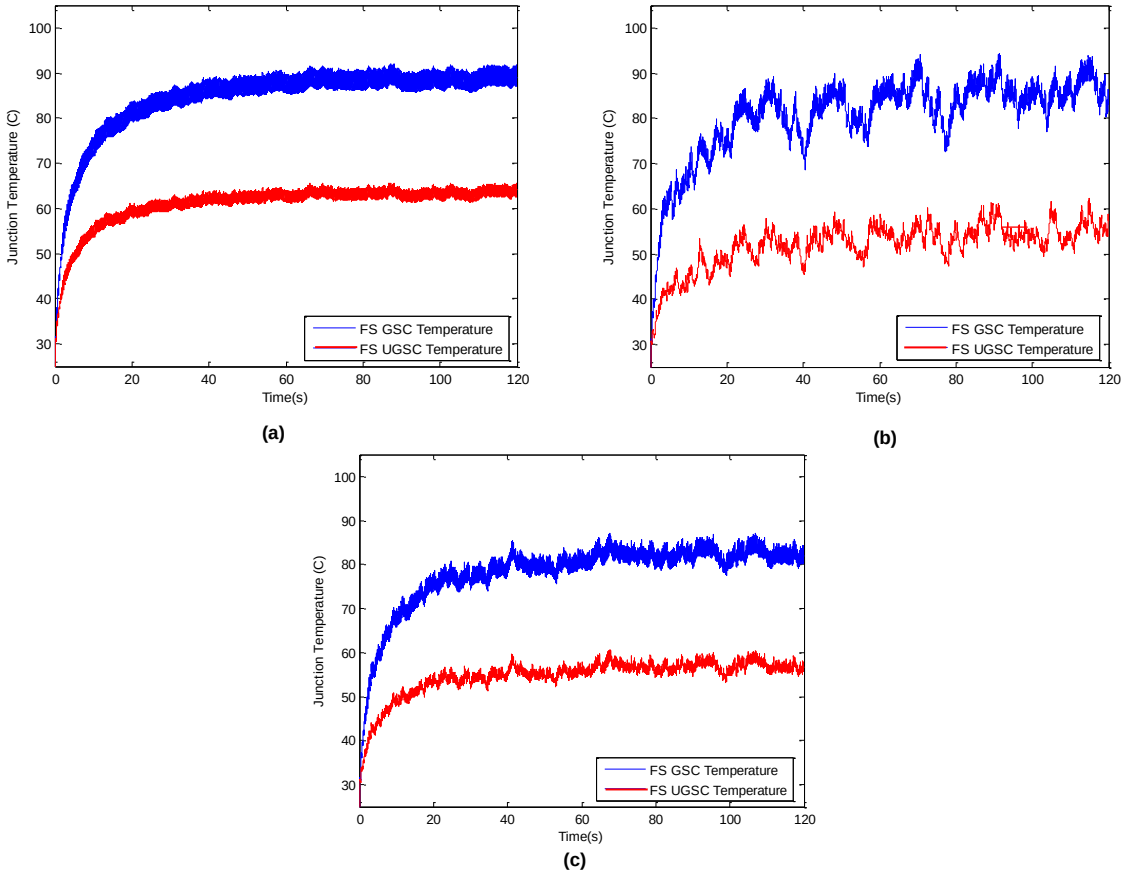


Figure 4.18. Temperature profile of FS based PECs with (a) conventional fixed DC link voltage; dynamic DC link (b) without and (c) switching frequency adaption schemes in generator side (GS) and utility grid side (UGS)

Temperature fluctuations, for variable DC link operation, are higher for the grid side converter devices due to the distorted DC link voltage and current injection. In fact, the mean temperature is approximately 25 °C lower than generator side converter which means the power modules will experience higher thermal stress caused by wind variations. Compared to FS topology, mean and peak temperatures of the converter modules are greater and more fluctuated for both generator and grid sides of PS topology, as seen in Figure 4.19 a–c. Maximum temperature fluctuation is approximately 12 °C at t = 80 s. Also, when frequency control algorithm is applied, mean temperature reaches to 92 °C.

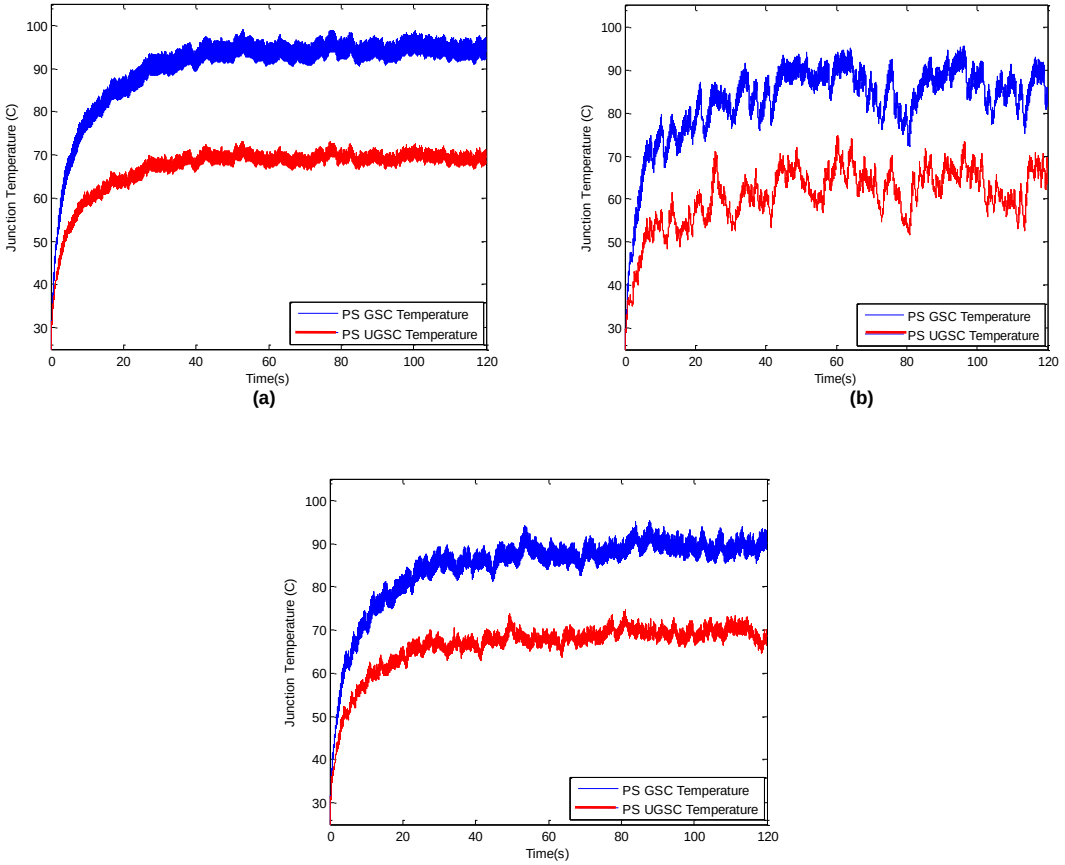


Figure 4.19 Temperature Profile of PS based PECs with (a)conventional fixed DC link voltage; dynamic DC link (b) without and (c) switching frequency adaption schemes in GS and UGS.

The temperature fluctuation however, is reduced by 9 °C which would reflect on the thermal stress induced during the operation. Similar to the FS converter topology, higher fluctuation (~15 °C) and lower mean junction temperature (~70 °C) profiles were estimated, on the GSC.

4.6.3 Thermo Mechanical Performance of Proposed Model

As a case study, FS generator side converters' power loss profiles of each three of the topological models were applied on top of the chips within FE analysis for obtaining the thermo-mechanical performances. Due to computational speed limitation in FEM, step time of loss profile was resampled into 5 ms range. Power losses were scaled by 1/12 factor; then were applied individually as boundary heat source on the each top surface of the silicon chip layer. This approach made it possible to locate thermal stress caused by thermo-coupling

heat effect across neighbour chips located on each substrate. Von Mises stress which occurred due to the power loss profile extracted from each topological operating approach are shown in Figure 4.20.

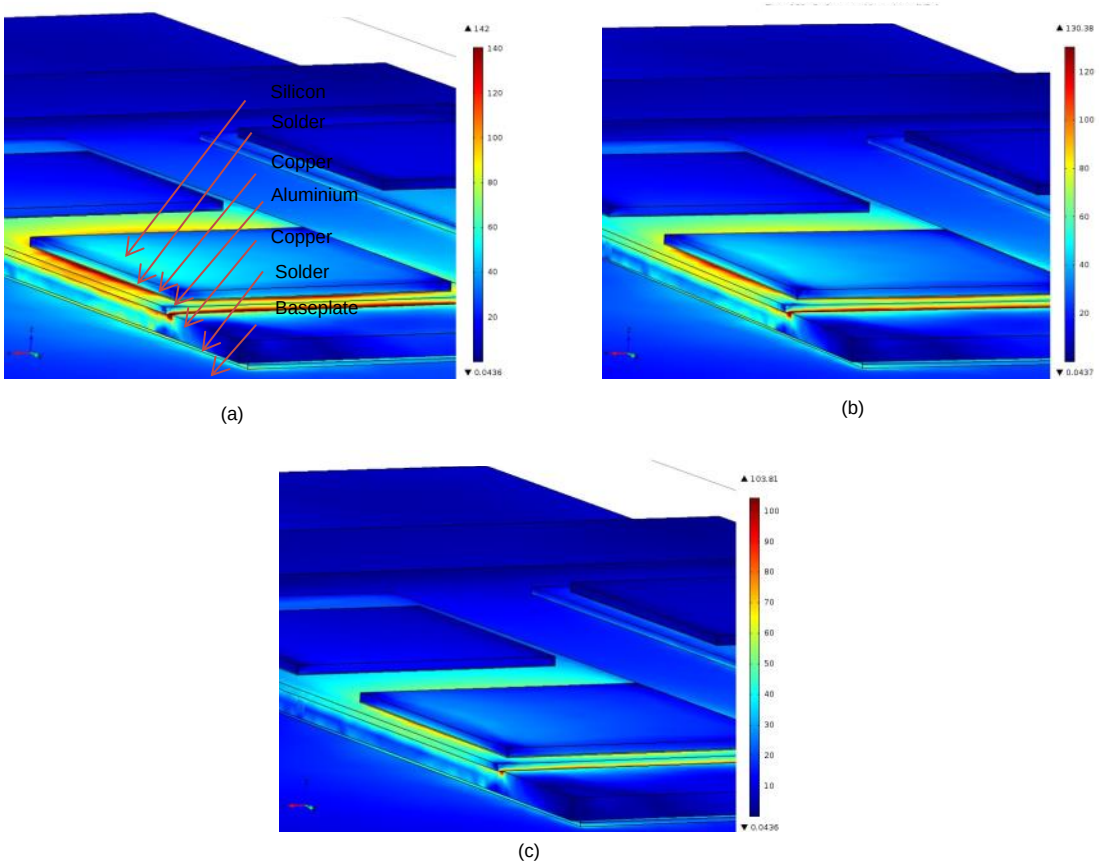


Figure 4.20 Surface von Mises stress for FS based BTB converter's generator side power module with (a) fixed DC link; (b) dynamic DC link without and (c) with switching frequency adaption

It can be commented that the most stressed regions are the solder of silicon and copper of baseplate layers. The maximum von Mises stress is estimated at the edges of copper layer as 142 MPa for the fixed DC link operation, as shown in Figure 4.20 (a). On the other hand, it is possible to reduce it around 130 MPa with dynamic DC link operation, as depicted in Figure 4.20 (b). The performance of the proposed model in terms of maximum stress is also shown in Figure 4.20 (c). Compared to dynamic DC link mode, approximately 27 MPa stress deduction was attained. The maximum stress was reduced approximately to 103 MPa which is lower than the yield strength of the copper [243]. Stress across silicon layer edges and baseplate is reduced in overall, especially around solder of neighbour substrates compared to dynamic DC link approach. First principle stress analyses are shown in Figure 4.21 (a)–(c)

for each topology. Most effected regions are middle edge of the silicon and aluminium ceramic layers. Proposed method showed better performance with total difference as lower as 36 MPa compared to the static and dynamic DC link operations. Total principal stress can be estimated as 56.6 MPa. Table 4.4 shows the thermo mechanical profile comparison among each PEC. Although dynamic DC link operation has lower mean junction temperature profile, thermal stress distribution is worse due its highly fluctuated characteristics, compared to proposed driving scheme.

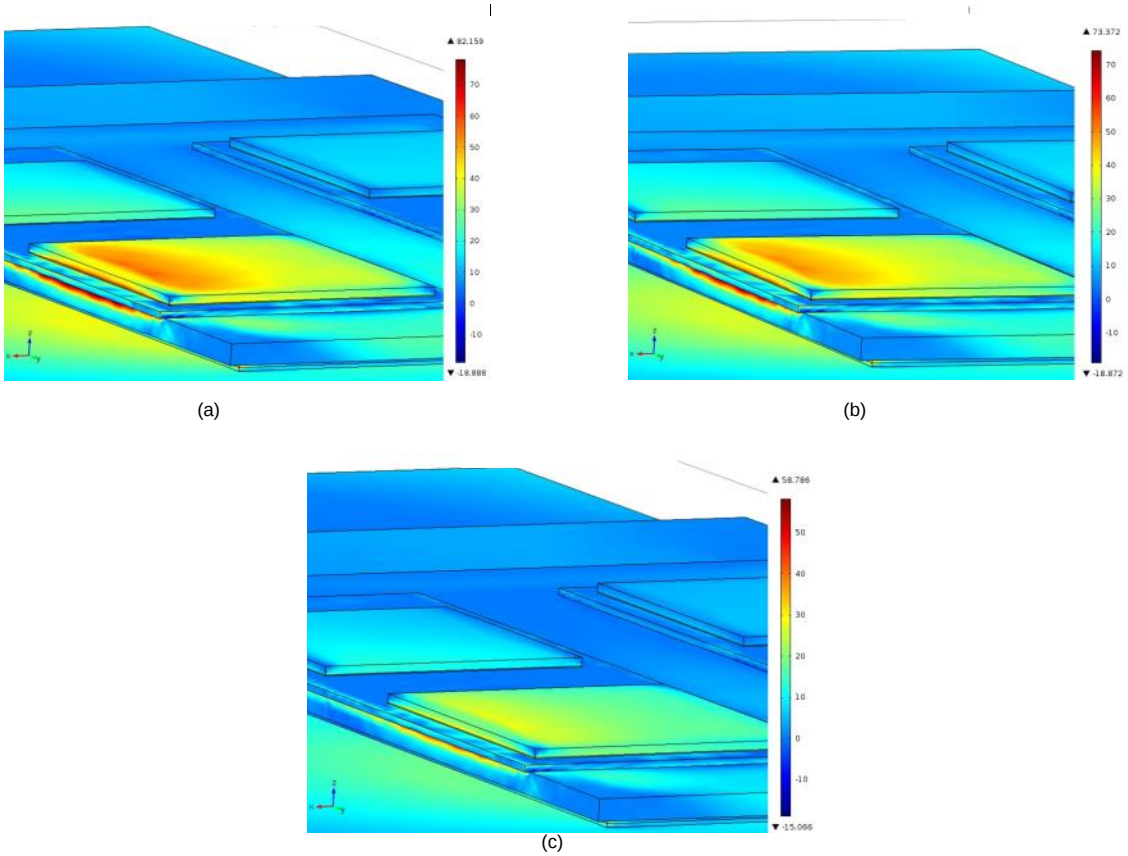


Figure 4.21 Surface first principle stress for FS based back-to-back (BTB) converter's generator side power module with (a) fixed DC link; (b) dynamic DC link without and (c) with switching frequency adaption

Table 4.4 Thermo mechanical profile comparison for each PEC

PEC Type	GSC			UGSC		
	Fixed DC Link	Dynamic DC Link	Dynamic DC Link & S. Frequency	Fixed DC Link	Dynamic DC Link	Dynamic DC Link & S. Frequency
Full Scale	142 MPa	130 MPa	103 MPa	93 MPa	81 MPa	64 MPa
Partial Scale	149 MPa	144 MPa	142 MPa	96 MPa	91 MPa	86 MPa

Total power losses with respect to mean and temperature fluctuations and stress for both FS and PS schemes are shown in Figure 4.22. It is seen that the proposed scheme showed

better performance for the FS based wind energy system. Mean junction temperatures are approximately lowered by 8 °C compared to the static DC link system for both GSC and UGSC. Temperature fluctuation is also decreased by means of 50% compared to the variable DC link operation which will be the major benefit for stress deduction. Although, the instantaneous power losses at peak point are decreased by 20% in DFIG system, this deduction did not reflect on mean junction temperature and maximum stress (~7 MPa in GSC,~10 MPa in UGSC) since the power absorption during sub-synchronous mode increases thermal cycling, unlike in FS topology. In spite of the highly cycling thermal profile, 5 °C mean junction temperature deduction is established compared to the conventional topology for both side converters of the PS based wind system model.

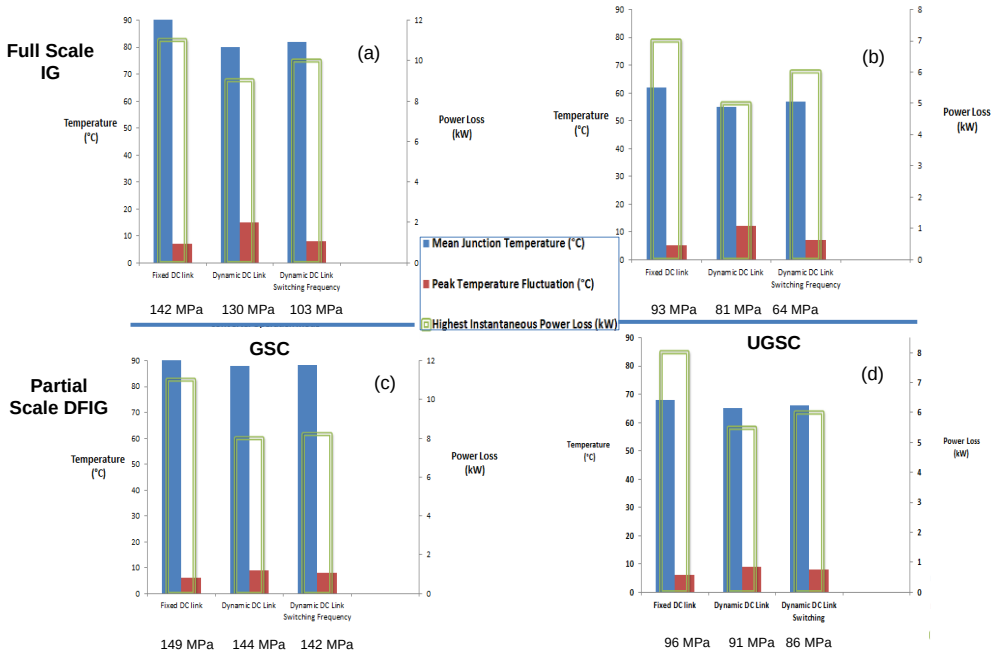


Figure 4.22 Overall thermo-mechanical and electro-thermal for (a,c) generator and (b,d) grid side power modules on FS and on PS doubly fed induction generator (DFIG) based BTB PECs.

4.7 Experimental Validation of Thermo Mechanical Model

The experimental validation of thermomechanical FE model and the proposed switching control method with variable DC link operation were achieved via dSPACE RTI by using a three phase inverter module; namely the FS10R12VT3 by Infineon Technologies. This device is a scaled down module of the FF1000R17IE4 which is constructed with six pairs of IGBT/Diode chips. It is more suitable to be tested under laboratory condition due to its low power capacity.

4.7.1 Physical Properties of the IGBT Inverter Power Module

Inverter module, FS10R12VT3, was purposely selected due to its low current characteristic and cost effective compact design. Its commercial name is EasyPACK 750, sixpack IGBT module with IGBT3. It was originally purchased in capsulated form as seen in Figure 4.23.

Figure 4.23 View of the FS10R12VT3 Inverter

Circuit configuration of the inverter module is shown in Figure 4.24. It consists of six IGBTs and six diodes. Unlike the previously studied Dynex DIM1200ASM45 single power module, the gate signalling should individually be supplied for each device. It is simply in the form of three parallel connected Infineon FF1000R17IE4 modules.

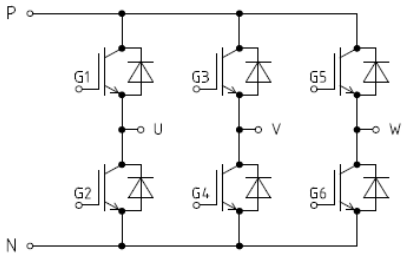


Figure 4.24 Circuit configuration of the FS10R12VT3 Inverter

The specifications of the module are presented in Table 4.5. As it is shown, the device has 1.2 kV maximum voltage and 16 A current capacities at 25 °C. The energy loss distribution over the device was calculated by a datasheet study using the methods studied in Chapter 3. Hence, the module losses were extracted to calculate the losses for each chip by using the eqn. 3.1.

Table 4.5 Specifications of the inverter module

Spec.	V_{CEs}	$I_{C(T=25C)}$	$I_{C(T=80C)}$	C_{ies}	C_{res}	$t_{d(on)}$	t_r	$t_{d(off)}$	t_f	$E_{on(T=25C)}$	$E_{off(T=25C)}$
Value	1.2 kV	16A	10A	0.70nF	0.026nF	0.037µs	0.02µs	0.29µs	0.09µs	0.95mJ	0.7mJ

The module was carefully de-capsulated by Dremel Corded Multi-Tool 3000 driller in order to locate the chip locations and appropriate thermal camera imaging during experimental tests. The internal view of the inverter module and the chip locations can be seen in Figure 4.25.

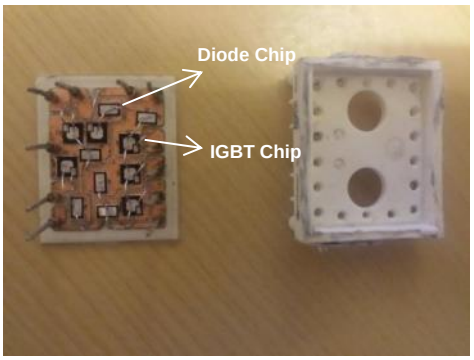


Figure 4.25 View of the de-capsulated FS10R12VT3 Inverter

The chips located in inverter module are attached on the substrate by lead-free soldering technique. This feature provides a possibility for a model based comparison study between lead containing and lead free solders, once the existed properties in FE are experimentally verified. The module does not contain a baseplate. Hence, it is mounted directly on an aluminium heat sink by thermal grease, namely the SK 100 by Fischer Electronic, in experiments and for modelling**.** An enhanced version of the driver circuit, presented in Chapter 3, was implemented in order to drive the inverter module. 3-phase/6-channel PWM feature of the DS5101 platform was used to generate gate signals. Then, the implemented driver circuit was used to increase to power level of these signals for sufficient gate driving.

4.7.2 Finite Element Model of the FS10R12VT3 Inverter

FE model of the inverter module was studied in details by using COMSOL. In order to increase the accuracy, dimension and material properties of each layer as well as the geometrical shapes of the wire bonds were accurately designed. The meshed view of the inverter model with the attached heat can be depicted in Figure 4.26. The geometry was modelled with 111743 tetrahedral elements. Mesh size for the heat sink and individual layers of the module are different for computational efficiency. Mesh refinement was completed by scale factor of two especially only for narrow edges of wire bonds and thin solder layers.

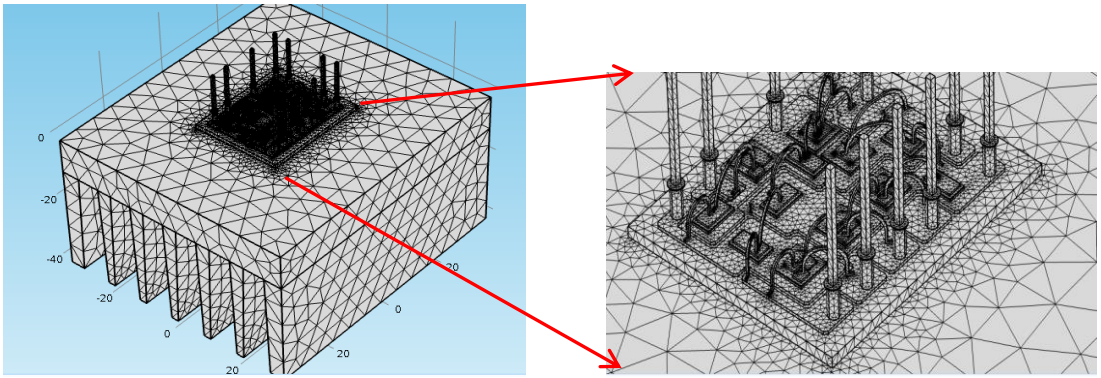


Figure 4.26 Meshed FE model of the FS10R12VT3 Inverter

In the model, thermal conductivity properties are defined as a function of temperatures and considered as dynamic functions. Please refer Appendix for the material specifications data sheet of the module. Similar to the previously modelled power modules, heat diffusion equation was defined for whole model to solve the distribution of temperature variations. As stated in previous section, the module was unmounted and the encapsulation silicone gel was removed. Hence, thermal isolation is no longer provided for the inverter module. In order to provide these test conditions in experimental analysis, the heat transfer coefficient h is defined as 5 W/m^2K over the model representing the natural convection. The ambient and heat sink temperatures were set to be 20°C. Each chip was heated, in individual simulations, by a constant two dimensional 10 W heat source. Heating operation for a Diode chip can be seen in Figure 4.27 (a) & (b) at top surface and middle of the chip, respectively.

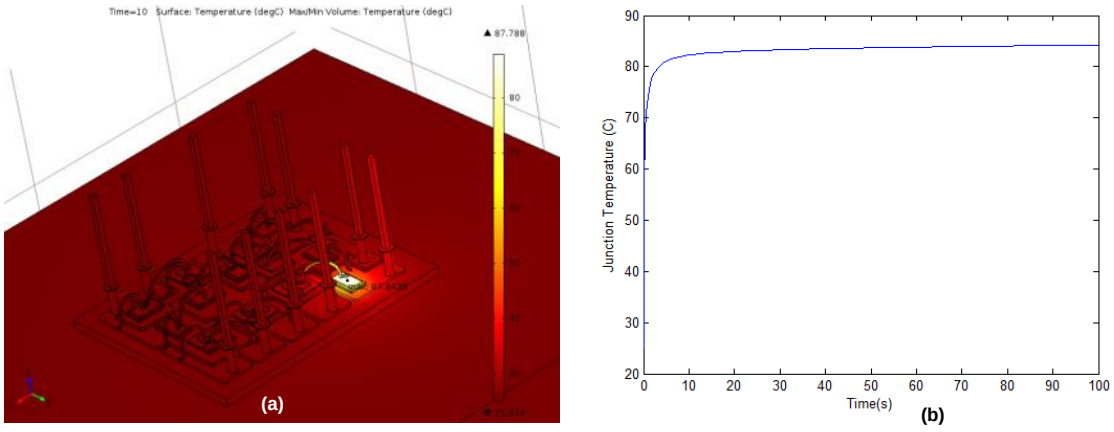


Figure 4.27 Heating operation of Diode chip of FS10R12VT3 Inverter at a) top surface and b) middle

In order to extract the thermal impedance parameters, the methodology defined in Chapter 3 was followed. Then, the thermal impedance matrix was implemented based on the self-heating and cross coupling heat generations among each neighbouring chips along with thermo mechanical modelling analysis.

4.7.3 Experimental Set-up

The heat sink, with dimensions of 75 x 66 x 40mm, was mounted on an isolated mica platform along with the driver circuits. In order to mount the input and output terminals of the inverter module, a PCB circuit was implemented and soldered to the specified legs. The inverter is isolated through the middle gap of the PCB circuit and mounted directly on the heat sink. The pin numbers and the design can be seen in Figure 4.28.

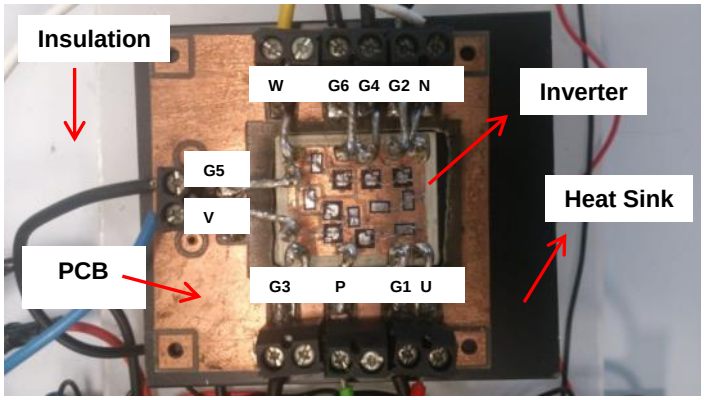


Figure 4.28 Inverter module design

Although, there are commercially available gate driver boards such as 2ED300C17-S recommended driver by Infineon (unit price £92.86 at RS), these solutions are commonly expensive. Therefore, the driver circuit is fabricated by the author as an extending version of the implemented design in Chapter 3. Compared to the previous case, a total of six gating circuits have been implemented for driving six individual gate signal provided by DS5101 DAC platform. The total cost is approximately £20 cheaper by considering the unit prices of the HCPL-4502 (£1.14) and TD351ID (£1.66).

4.7.4 Multisim Model Filter Design

Multisim software was used at this part of the research for filter design of the three phase inverter since it contains actual circuit components compared to the generic ones in Simulink. This is useful during the modelling process before purchasing the physical filter components. The aim of this chapter is not to design an optimised filter for the inverter module. Nevertheless, for accuracy of the RT electro thermal measurements, appropriate current and voltage signals are needed in terms of harmonic distortion. A conventional, second order LC filter was implemented to reduce harmonic distortions caused by fundamental square waved output voltage of the inverter. A shunt capacitor is used to further attenuation of the switching frequency components [250]. It is selected to produce low reactance within the control frequency range. The resonant frequency is calculated from eqn. 4.35.

$$f_o = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{LC}} \tag{4.35}$$

where the L is the inductance, C is the capacitance at selected switching frequency f_o. The characteristic impedance of the passive filter Z is given by:

$$Z = \sqrt{\frac{L}{C}} \tag{4.36}$$

The impedance, Z determines filtering performance at harmonic frequencies except for the resonant frequency. Lower characteristic impedance reflects a lower DC capacitor voltage as well as lower EMI emissions [251]. The modelled 3-phase inverter systems can be depicted in Figure 7.7. As filtering, 10 mH inductors and 33µF capacitors were selected along with the available 18 Ω resistors and 10µF capacitors as balanced loads.

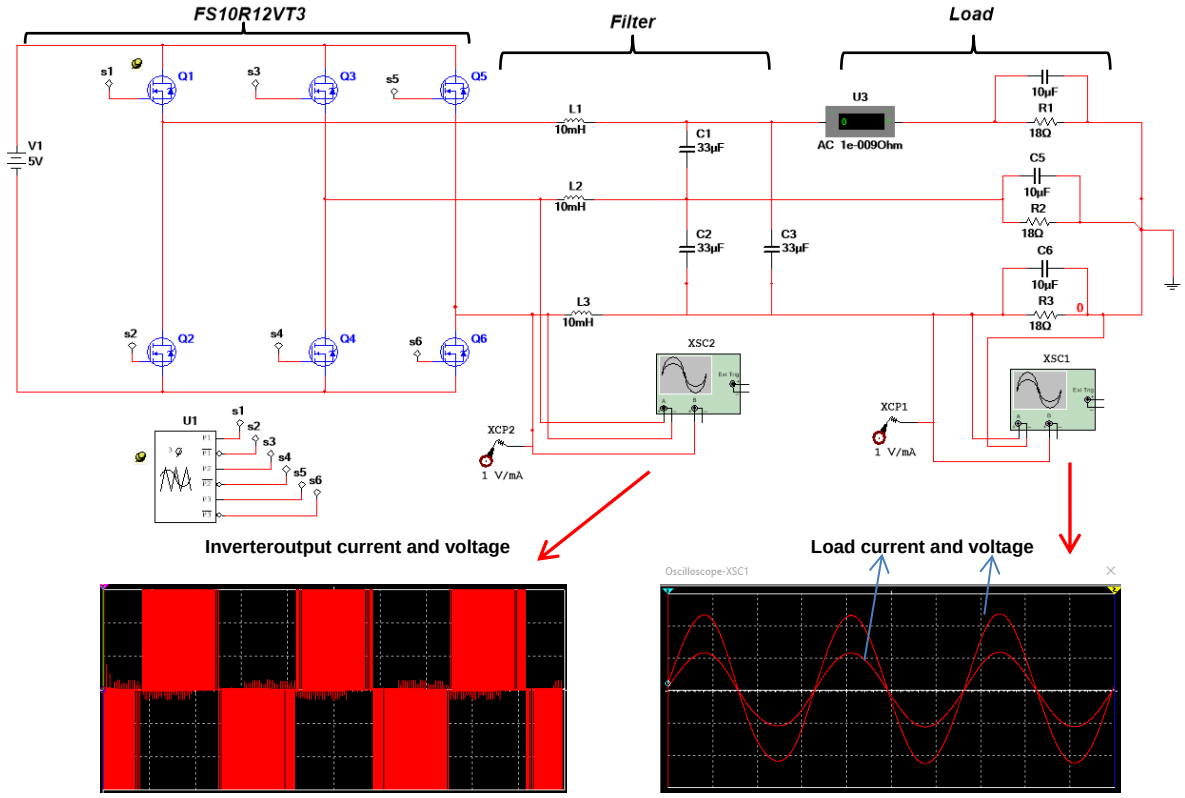


Figure 4.29 View of the Multisim Model

As it can be seen from the Figure 4.29, low distorted current and voltage signals are obtained with the selected filtering. However, if the filter was designed with a 10 µF capacitors and 1 mH inductors, the load current and voltage signals would have been highly distorted, as shown in Figure 4.30.

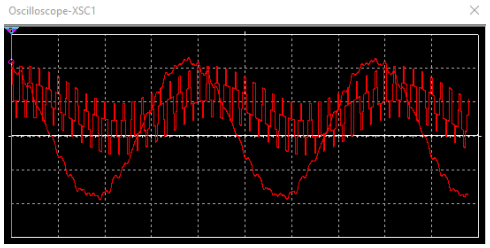
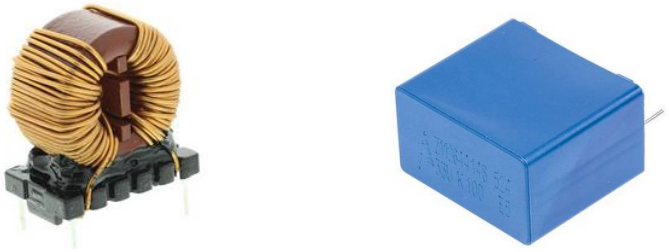


Figure 4.30 Load Current and Voltage

4.7.5 Real Time Implementation of Experimental Setup

The filter inductor was selected as leaded type since it is applicable to power line output filtering systems without a stable ground connection. It is namely the 10mH WE-CMB HC by Wurth Electronic. It has the maximum current capacity of 5A and ±30% impedance tolerance. On the other hand, the filter capacitor was purposely selected as through whole

polyester film capacitor type. This type is particularly manufactured as AC filter capacitor and it is namely the B32524 AC capacitor by Epcos. It is 33µF (±10%) with the voltage levels of 100 V for DC and 63 V for AC applications. The physical view of the filter inductor and capacitors can be seen in Figure 4.31 (a) & (b), respectively.



(a) (b)

Figure 4.31 a) Filter inductor and b) capacitor

The load side was implemented as three-phase balanced resistive/capacitive load with the 10µF version of the Epcos B32521 AC filter capacitor and an axial leaded 18Ω, 50 W, ± 5%, resistor namely the WH50-18RJI by Welwyn, is physically shown in Figure 4.32.

Figure 4.32 Load Resistor

The view of the implemented inverter systems can be seen in Figure 4.33.

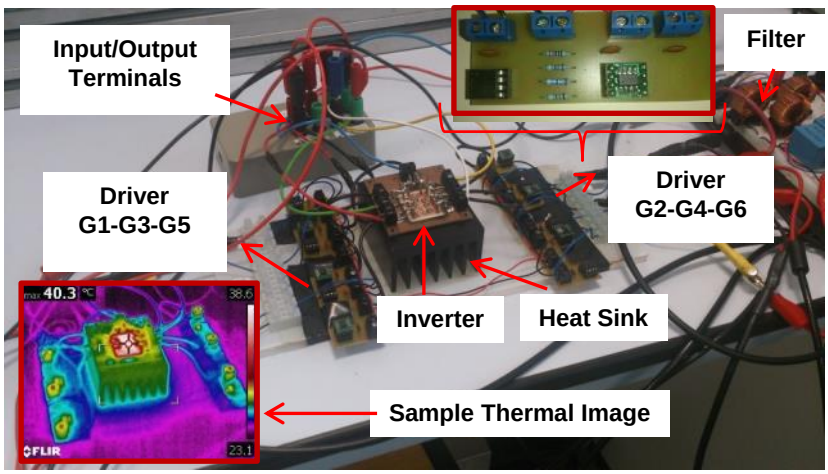


Figure 4.33 Physical view of the inverter systems

The DS5101PWM6 block from dSPACE Control desk was used to generate SPWM based gate signals for each IGBT as shown in Figure 4.34. The load current and voltages were captured by the DS2004 A/D platform and processed in to power loss and thermal models. A case study was conducted at constant 5V volt input while the switching frequency of the SPWM was 100 kHz. Different filters were applied to verify the Multisim modelling experimentally.

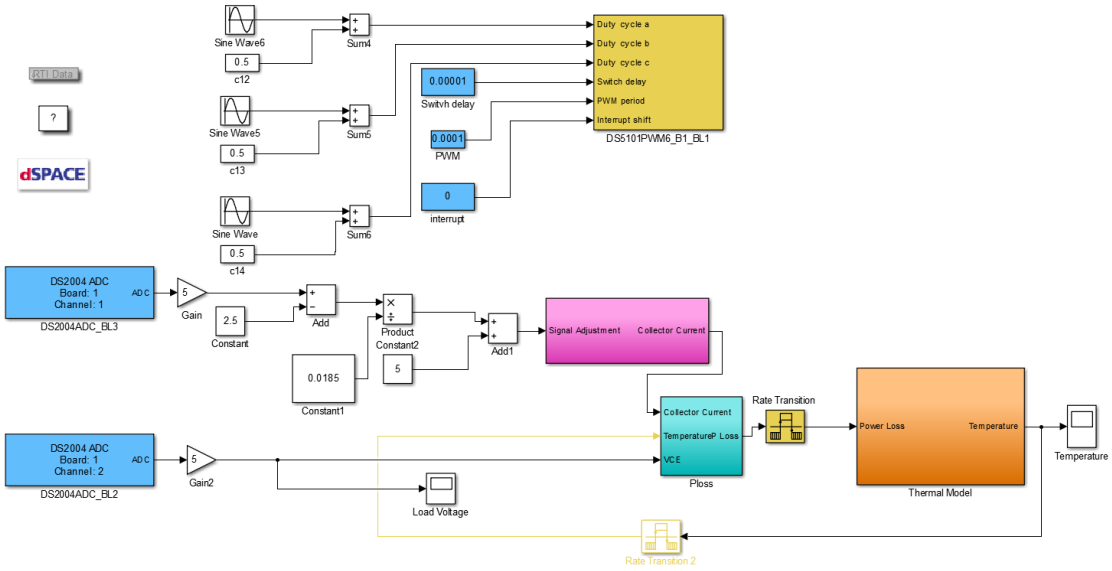


Figure 4.34 dSPACE implementation

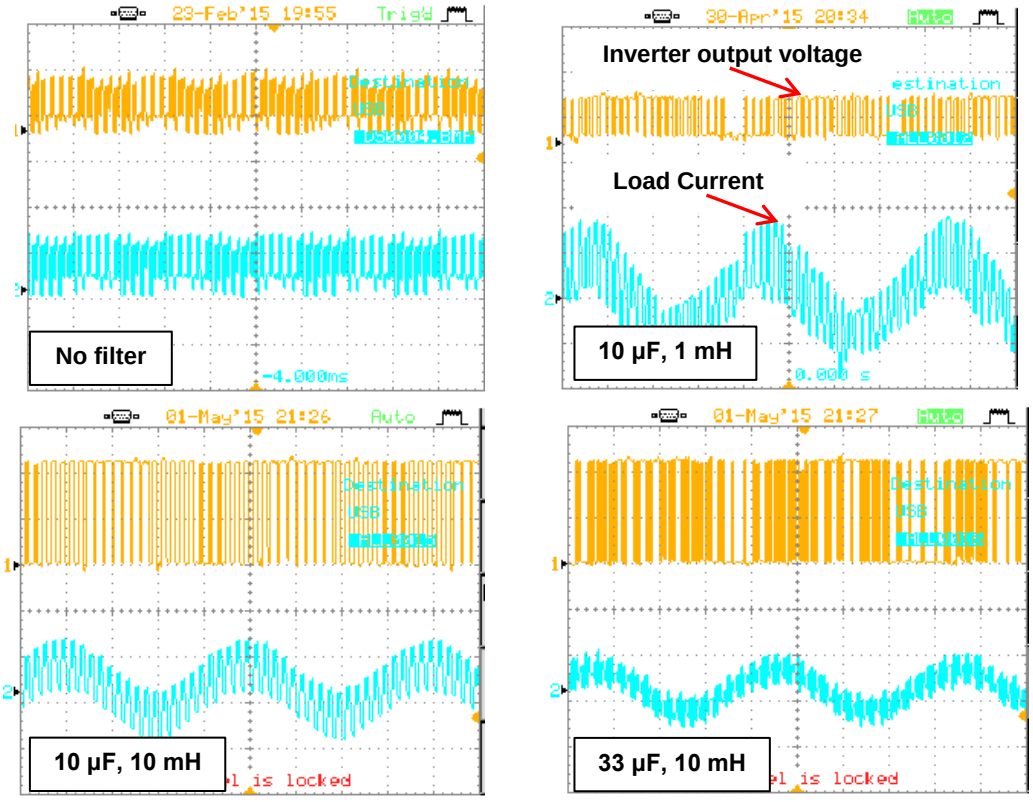


Figure 4.35 Experimental converter output voltage and load current signals

Much smoother current-voltage characteristic is obtained by using the 33µF-10mH filter as depicted in Figure 4.35. The results for the Multisim simulation are also verified in terms of oscillatory load current for the case where the 10µF - 1mH filter is used. Although, the 33µF-10mH filter is more expensive compared to the other choices, it was used for the rest of the experimental work in order to increase the accuracy of temperature monitoring.

4.7.6 Thermo Mechanical and Thermal Model in MATLAB/Simulink

The electro thermal and the thermo mechanical modelling methodologies derived previously were applied to the inverter module by considering self and coupling effect among each chip. IGBT and freewheeling diode current and voltage signals are directly embedded in power loss models for each device. The temperatures for each layer were monitored by feedback look through individual thermal layer model. View of the Simulink electro-thermal model can be found in Appendix. Results are depicted in Figure 4.36 (a) & (b) for simulated and experimental studies, respectively.

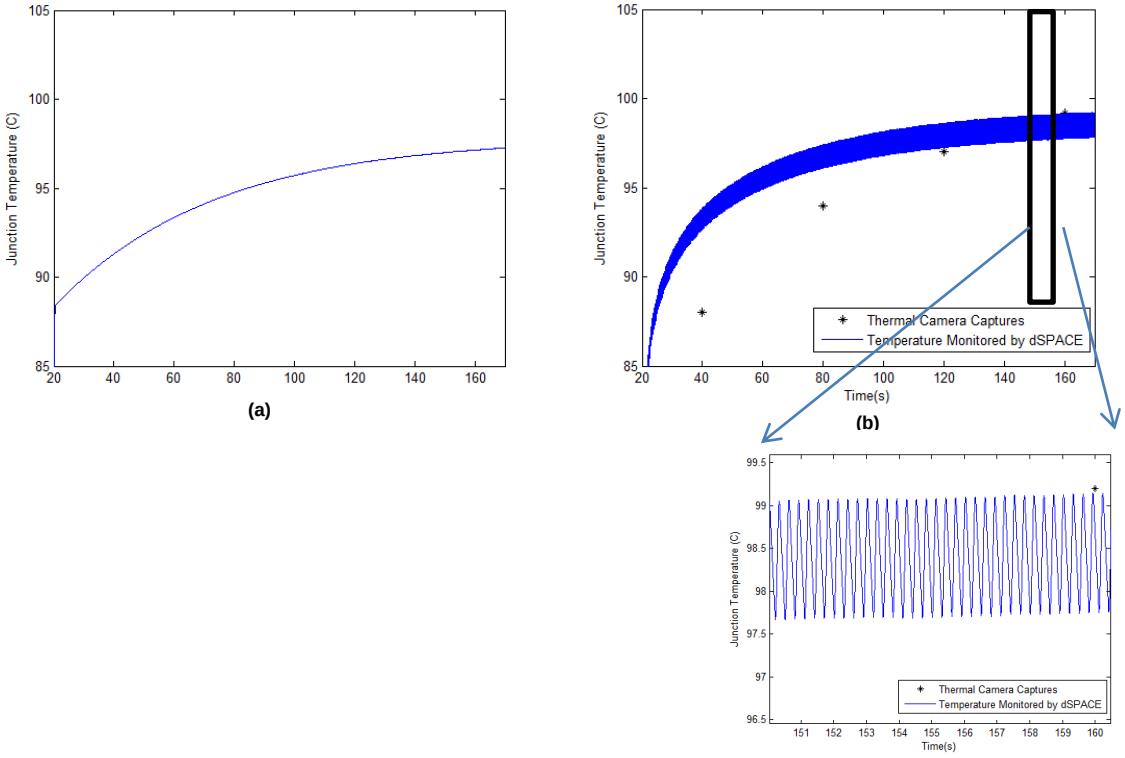
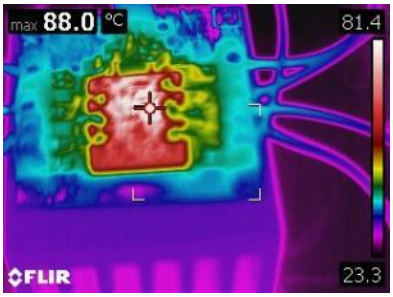
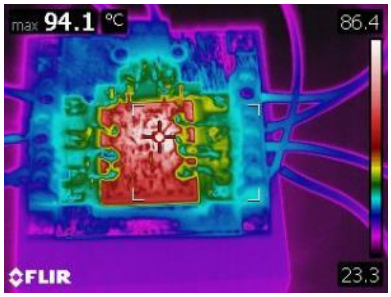


Figure 4.36 Temperatures observed by (a) Simulink model and (b) by dSPACE and thermal imaging

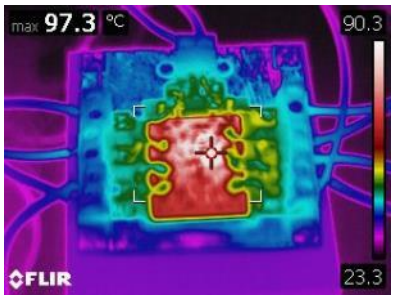
The input DC voltage was adjusted as 5V where the switching frequency was 50 kHz. Input current signals were captured through the output of the inverter terminals. Then, these signals was recalculated for representing sinusoidal IGBT and diode currents with 120° degree phase shift among them. The maximum temperature reached up to 96 °C for the simulated case. Compared to the individual heating operation, by the electro thermal model in Simulink, 15°C temperature increase can be obtained by considering the heat coupling effect. The experimental results are also in good agreement with the simulated data as seen in Figure 4.36. The thermal imaging captures were taken in 20 seconds of intervals (see Figure 4.37) while the dSPACE model predicts the instantaneous temperature based on the load current and voltage. Approximately 1.5 °C temperature swing was estimated during the inverter operation, as well.



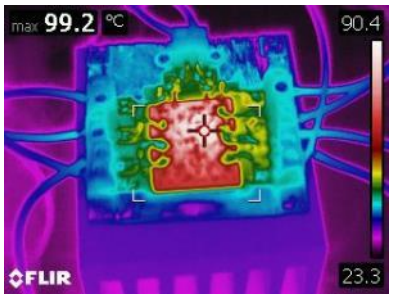
(t=40s)



(t=80s)



(t=120s)

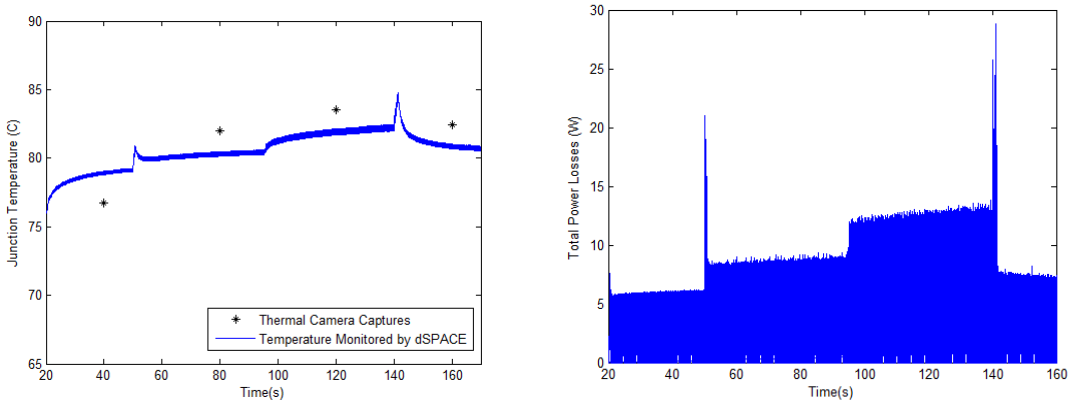


(t=160s)

Figure 4.37 Thermal camera captures

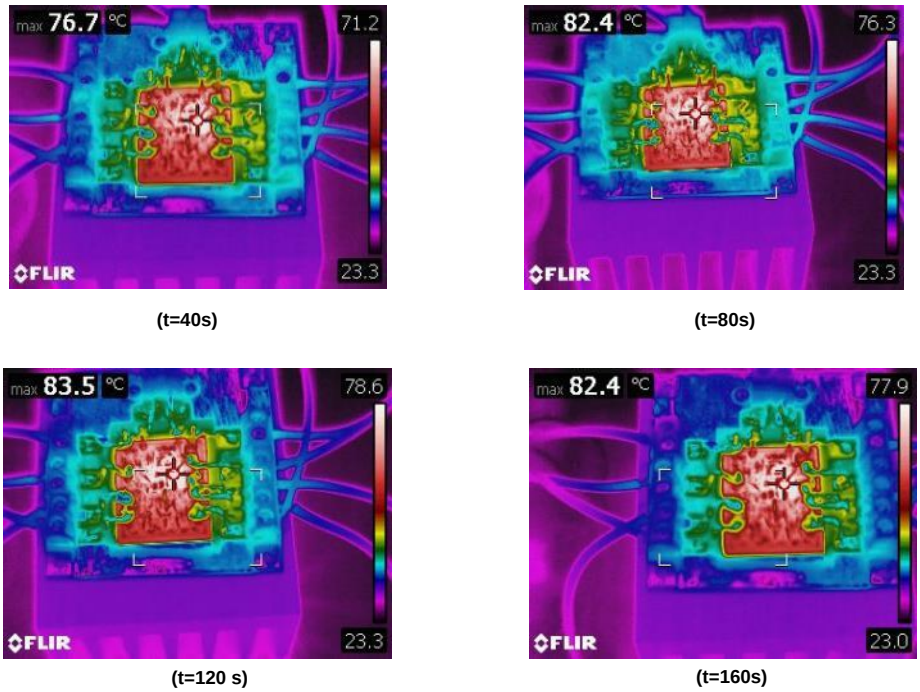
4.7.7 Variable Switching Frequency Operation

A variable temperature profile was generated by varying the switching frequency at constant input voltage. Please, refer to the Appendix for the dSPACE Control Desk view of the generated study. Four sets of different SPWM switching frequency were applied to the inverter in 20 seconds intervals. The trends of increasing/decreasing intervals were kept similar to the variable frequency set of data in Section 4.6. The monitored temperature along with the power loss data can be in Figure 4.38 (a) & (b), respectively during variable switching frequency operation. The initial switching frequency was 10 kHz and it was increased to 50 kHz and 100 kHz in each 20 seconds. Then, the frequency was pulled back to 20 kHz at 140 seconds. The power losses increased as the switching frequency increased and this reflected on the instantaneous temperature where it was at its highest, 83 °C at 100 kHz. Thermal camera captures in stated time intervals can be seen in Figure 4.39.



(a) (b)

Figure 4.38 (a) Temperature observed by dSPACE and thermal imaging, (b) power losses



(t=40s) (t=80s)

(t=120 s) (t=160s)

Figure 4.39 Thermal camera captures

By the experimental results, it can be commented that the argument of proposed method and model based studies in Section 4.3 are verified in terms of switching frequency variation and its effect on the temperature changes. The higher switching frequency led higher power losses at specified time intervals which caused temperature increments and vice versa. The distortion of the output voltages at various switching frequency rates also explains the total harmonic distortion variations where it was the highly fluctuating at 10 kHz of switching

frequency and was smoother as the switching frequency increases up to 100 kHz as shown in Figure 4.40.

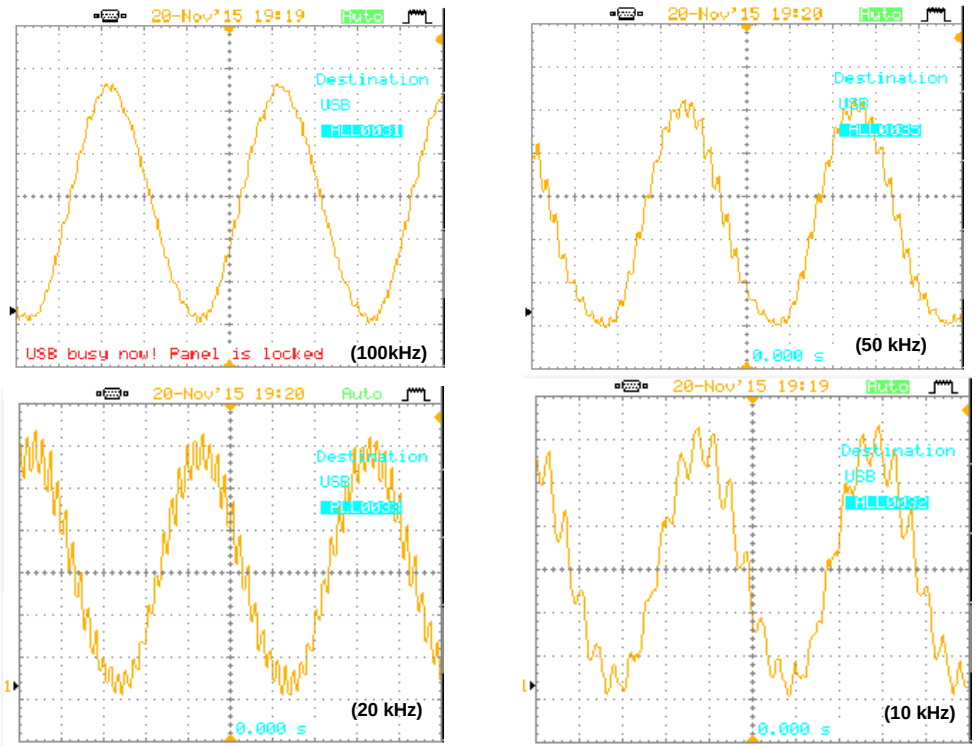


Figure 4.40 Load voltages at different switching frequencies

During the variable switching frequency operation, as the switching frequency deceases, the temperature and thermo mechanical thermal stress decline. However, the signal distortions occur due the lowered switching frequency which increases the total harmonic distortions.

4.8 Summary

A switching frequency solution to minimise thermal effects and the induced stress of PECs was demonstrated in this chapter. Based on the previously discussed literature survey, there is very few study which dealt with the thermo mechanical stress variation on the PECs during changing environmental conditions. Promising results were achieved by optimising switching frequency of PECs within dynamic DC link voltages for wind energy applications. The proposed adaptive switching driving scheme managed to control the total power losses of a two level back-to-back converter platform used in full scale (FS) and doubly fed

induction generator (DFIG) based partial scale (PS) wind systems. Moreover, the IGBT junction's mean temperature and the induced stress were eliminated and kept within acceptable levels, which in turn maximise the life cycle of such PECs as it will be presented in the following chapter. With the proposed approach, "the total temperature fluctuation" was notably reduced; for FSIG by 12 °C, DFIG by 5 °C. Such temperature reduction leads to a total stress decrease by about 27 MPa. The drawbacks associated with the proposed model are related to its complexity, possible current and voltage fluctuations which may cause increase to the total harmonic distortion fed into the utility grid as discussed in [252]. The variable frequency could also forces the DC-link capacitor and cause decrease in the expected total lifetime to failure which would cause further replacement cost. This issue can be solved by active filtering techniques [251]. The switching frequency control methodologies were verified by an accurate implementation of physical DC/AC inverter. An actual wind turbine system was used to apply variable speed operation and to find its effects on the thermal behaviour of the coupled inverter system. Good agreement was obtained with the model and experiment based studies. The reliability of the inverter due to the fluctuated thermal profile is also expressed and the higher speed operation caused more stress and life time consumption based on the experimental work.

Chapter 5

Lifetime Modelling of Power Electronic Modules

5.1 Overview

Reliability modelling for the switching devices used in power electronic converters is presented in this chapter. The electro thermal and thermo mechanical models implemented in previous chapters are further extended for calculating life time estimation of the PECs. In addition to the thermo mechanical stress analysis in previous chapter, the advantages of the proposed variable DC-link and dynamic switching frequency control method on the lifetime of the PECs used in wind energy systems are verified. For this purpose, solder breakdown mechanism was considered as failure criteria.

A further case study was applied to an actual permanent magnet generator based wind turbine system test rig. A double bridge AC/DC rectifier was used to convert the generated AC power into DC. Then, the FS10R12VT3 was used as an inverter during variable environmental conditions in order to analyse the performance of the reliability of the bond wires located on IGBT and diode chips.

In order to extend existing studies in literature [211], [218], [221], in the final part of this chapter, the effects of Incremental Conductance (IC) and Perturb and Observe (P&O) maximum power point tracking algorithms on thermal stresses and reliability of PEC modules were investigated in a PV system based case study. By implementing a PV model, the associated MPPT algorithms and realistic electro thermal model of power electronic module's switching component (IGBT) used in a DC-DC boost converter was experimentally attached to a physical PV panel and real time temperature monitoring was interfaced with dSPACE. Temperature variations of IGBT were determined when IC and P&O algorithms were applied as MPPT method and these profiles were used in reliability models for lifetime consumption estimation.

5.2 Lifetime Analysis

Lifetime analysis for power electronic devices are evaluated by using Weibull statistics [183]. Devices under test are examined for determining the number of cycles to failure. Reliability of the PECs mostly depends on the associated switching elements (IGBT) since they are the most easily damaged components [127], [253] . The failure occurs due to the thermo mechanical stress caused by different thermal expansion characteristics of materials among

the IGBT package during temperature changes. The failure mechanisms of these devices are related to the cycling load of the module. Therefore, temperature profile of the IGBT was considered for estimating power cycling lifetime in terms of mean and cycling temperature. In order to relate the failure mechanisms and quantified reliability performance analytical models are developed to predict the lifetime such as [183]:

Coffin-Manson Model:

$$N_f = \alpha(\Delta T_j)^{-n} \tag{5.1}$$

This life time model takes the fluctuation of junction temperature, *ΔTj* into account. The *α* and *n* are constants, acquired experimentally.

Coffin-Manson-Arrhenius Model:

$$N_f = A(\Delta T_j)^{\alpha}.e^{\left(\frac{E_a}{k_b.T_m}\right)} \tag{5.2}$$

This model takes also the mean junction temperature, T_m into account where *K* is the Boltzmann constant and *Ea* is activation energy parameter.

Norris-Landzberg Model:

$$N_f = A.f^{-n_2}(\Delta T_j)^{-n_1}.e^{\left(\frac{E_a}{k_b.T_m}\right)} \tag{5.3}$$

This model is based on eqn. 5.2 and additionally takes the cycling frequency *f* of the junction temperature into account.

Bayerer Model:

$$N_f = K.(\Delta T_j)^{-\beta 1}.e^{\left(\frac{\beta_2}{.T_m}\right)}.t_{on}{}^{\beta 3}.I^{\beta 4}.V^{\beta 5}.D^{\beta 6} \tag{5.4}$$

This model considers a number of parameters where, the t_{on} is the heating time, I is the applied DC current, D is the diameter of the bond wire, and V is the blocking voltage.

5.2.1 Lifetime Analysis Verification for the PECs in wind energy systems

Thermal stress distribution for the chip solder layers of the Infineon FF1000R17IE4 power module was analysed in Chapter 4, for wind energy applications. Von Mises stress analyses was performed in order to calculate the average thermal stress on the module caused by three different operation modes of the power electronic conversion schemes. A conventional partial scale wind system with constant DC link voltage caused 150 MPa stress while this was decreased to 144 MPa with the variable DC link voltage. Also, a technique was studied in order to control the switching frequency within the variable DC link operation which led to 140 MPa average thermal stress. In this section, lifetime consumption analysis was conducted for the chip solders joints, based on the cycle to failure models studied by Ma et al. [1]. The model states that the expected number of cycles to failure for the solder can be derived as:

$$N_f = 1.4 \times 10^{16}.\Delta T_j^{-6.} \tag{5.5}$$

Model based solder temperature profiles for three operating modes are shown in Figure 5.1. In order to achieve total life consumption (TLC) caused by the combined effect load profile, Palmgren-Miner linear damage accumulation rule [254] was applied and modelled for failure prediction. It can be expressed as:

$$LC = \sum_{i=1}^{j} \frac{n_i}{N_i} \tag{5.6}$$

where n_i is the number of cycles, N_i is the measured lifetime in the i_{th} profile and j is the total number of load profile. The rule states that failure happens when condition TLC=1 occurs.

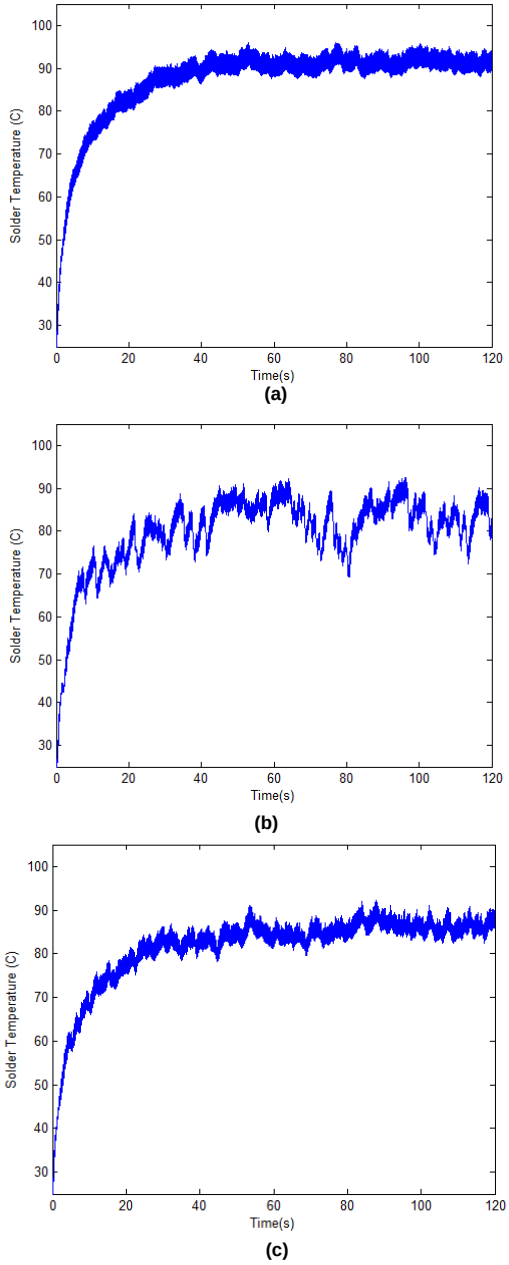


Figure 5.1 Solder temperature profile for different operating modes (a) fixed DC link; (b) dynamic DC link without and (c) with switching frequency adaption

Counting algorithms enable the evaluation of temperature cycles with an empirical lifetime model [137] by extracting the temperature cycles within the load-profile and storing in a data vector. The Rainflow method is one of these methods [255] for counting the temperature cycles. For lifetime estimation analysis purpose, Rainflow counting algorithm tool [256] was used to evaluate the temperature variation profile for the solder layer.

Rainflow algorithm was used to find the total number of thermal cycles for each data. Then, by using the life time estimation method, derived in eqn. 5.5, the TLC was calculated for each profile. The results are depicted in Figure 5.2.

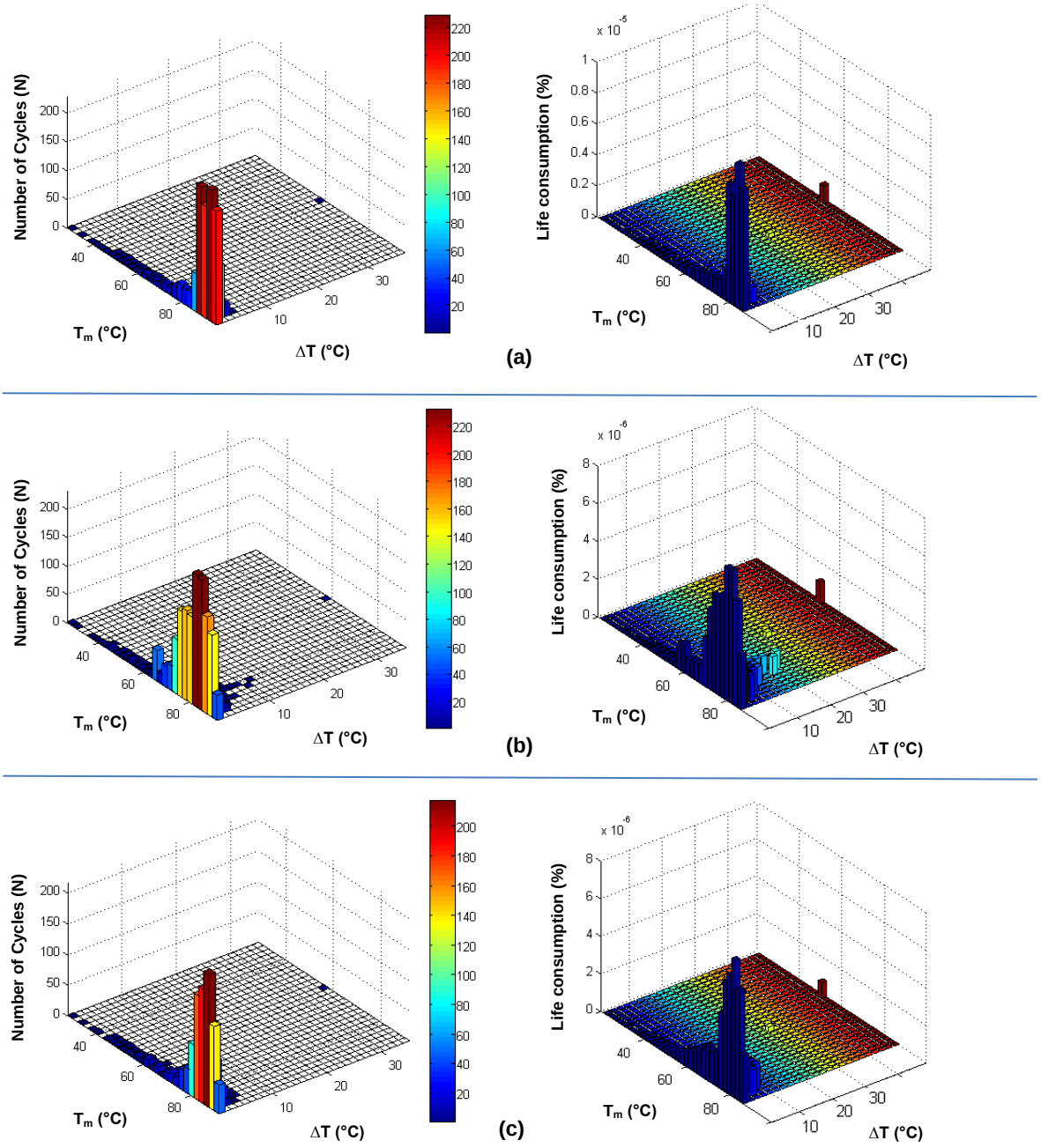


Figure 5.2 Number of Cycles and Life time consumption for PS PECs (a) fixed DC link; (b) dynamic DC link without and (c) with switching frequency adaption

As it is shown in Figure 5.2, the maximum life consumption for the solder in the fixed DC link operation was reached up to 1 x 10^{-5} at 80 °C. The TLC was 4.25 x 10^{-5} for the fixed DC link operation. With the dynamic DC link operation, the TLC slightly decreased to 4.06 x 10^{-5}. It

can be seen from the Figure 5.2 (b) that although the maximum consumption declined at most of the mean temperature points, the increment in temperature fluctuations (10°C <ΔT<20 °C) led insufficient TLC improvement for solder in variable DC link operation. With the proposed switching frequency control method embedded with variable DC link operation showed better TLC improvement especially by eliminating high temperature fluctuations. The highest and maximum cycles, 210, was observed at 78 °C mean temperature which caused 6 x 10^{-6} life consumption. The TLC for this method was calculated as 3.26 x 10^{-5} which is approximately 1x10^{-5} less compared to the other both methods. The thermal stress analyses, obtained in Chapter 4, are also in good agreement with the related TLC results. The highest average stress occurred for the fixed DC-link operation which caused higher TLC and vice versa for the proposed switching frequency control method.

5.2.2 RTI of Reliability Estimation of FS10R12VT3 Inverter at Variable Wind Speed

For the verification of the variable wind speed operation, a permanent magnet based 18 Watt, 1150 rpm wind turbine; namely the 910 MKII by Rutland was used. The physical view of the turbine can be seen in Figure 5.3.

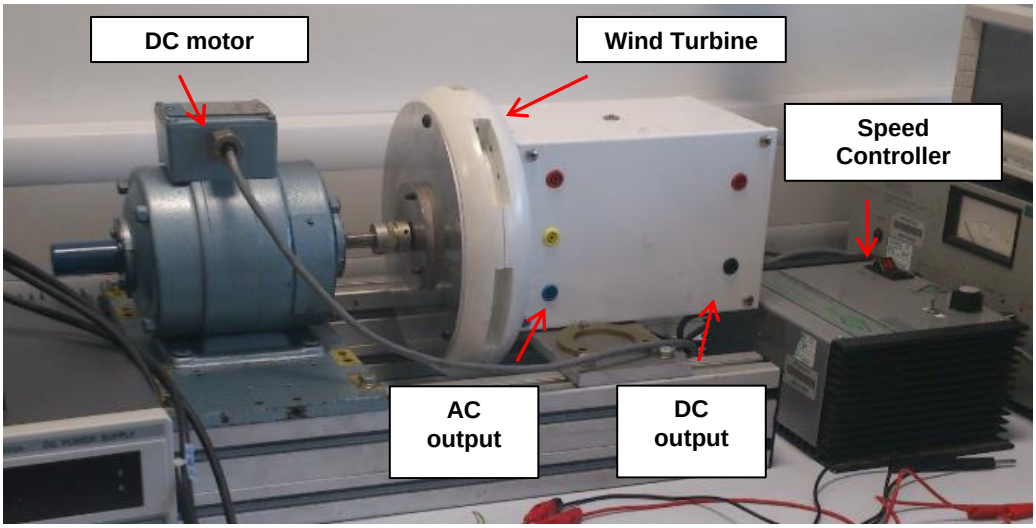


Figure 5.3 Experimental Set up

The speed of the wind turbine generator was adjusted by a DC motor which was attached to the centre hub of the turbine by a shaft. The motor is shunt type DC motor from NECO, at rating current of 0.75 A at 1500 rpm. A speed controller namely was used to derive the DC

motor; hence to control the speed of the turbine. During the experiment, the blades were purposely removed. The turbine output AC power was rectified initially by using two bridge rectifiers (KBPC3504) as shown in Figure 5.4.

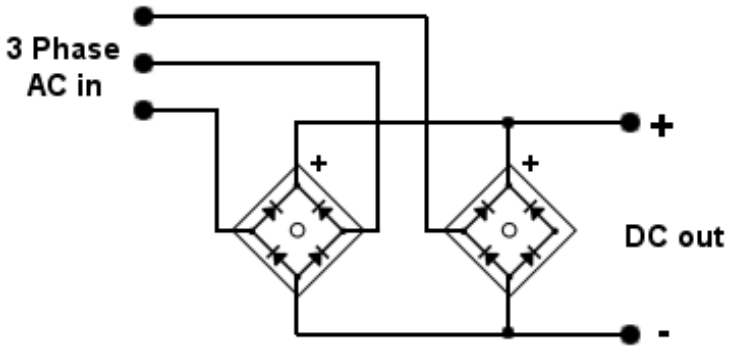
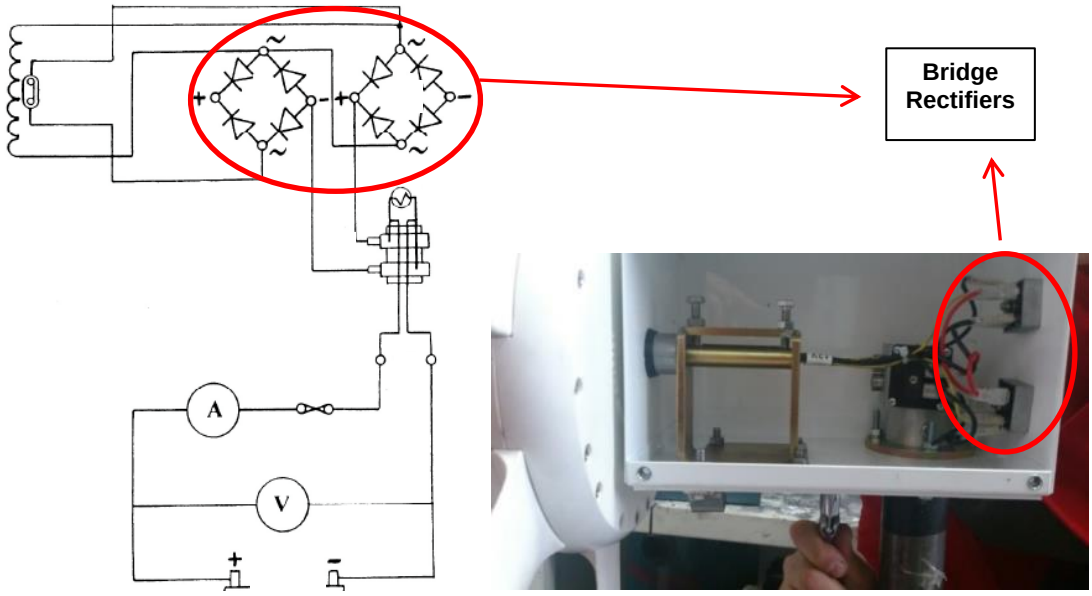


Figure 5.4 Two bridge rectifier

Internal scheme and physical view of the turbine hub can be seen in Figure 5.5 (a) & (b).



(a) **(b)**

Figure 5.5 (a) Internal schematic and (b) physical view

The speed controller has ten sets of speed range. The turbine speed was controlled by this portion in order to represent a variable wind profile. The output AC power was firstly rectified by the specified bridge diodes. Then, operating at constant switching frequency,

the FS10R12VT3 Inverter was coupled with the rectifier output in order to produce three-phase power. The filter and load components were identical with the previously designed system in this chapter. The gate signals were provided by dSPACE and the load current was used to predict inverter temperature during the variable speed profile. The applied speed range profile can be seen in Figure 5.6 (a) along with temperature variations in Figure 5.6(b).

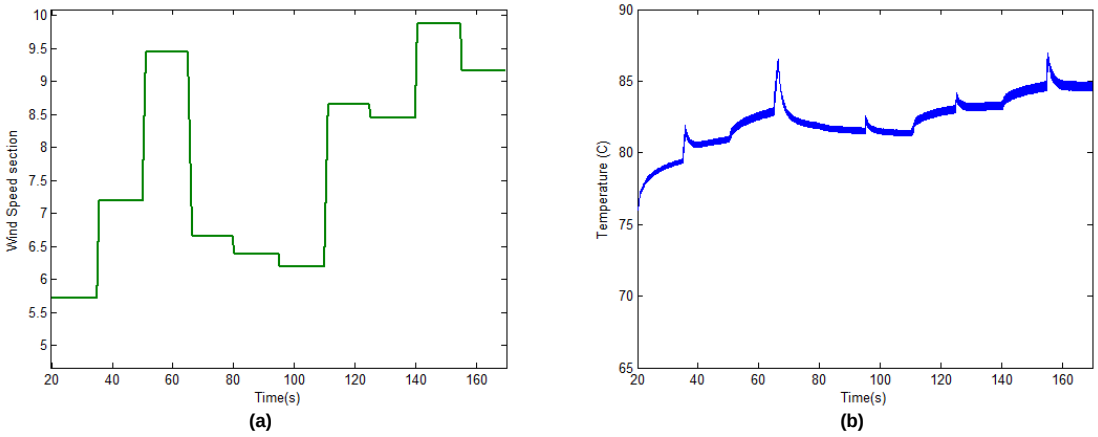


Figure 5.6 (a) Speed and (b) Inverter Temperature

As it is seen from the Figure 5.6, the increase in the wind speed caused temperature increment for the Inverter. The highest estimated temperature was 85 °C at the speed portion 10. The thermal profile behaviour with respect to the wind speed changes defined and modelled in Chapter 4 are verified based on the experimental case study. It can be stated that during the wind speeds increment, the temperature profile of the PECs are increases. In this condition, by lowering the switching frequency, the thermal stress can be decreased as a result of the analysis in previous chapter. For further verification, a study was completed for the life time prediction of the inverter module under variable wind speed operation. The thermal data for the inverter was defined by AC input currents. Lifetime modelling study, defined in previous section, was applied to processed temperature data to count number of thermal cycles and then for predicting the total life consumption (TLC) for aluminium wire bonds. The model of the number of total cycles to failure during a thermal cycling on wire bonds studied by Ma et al. [1] was used. It is defined as:

$$N_f = 4 \times 10^{17} . \Delta T_j^{-6.48} \tag{5.7}$$

Based on the Rainflow counting algorithm analysis [256], the total temperature cycles data was calculated as seen in Figure 5.7.

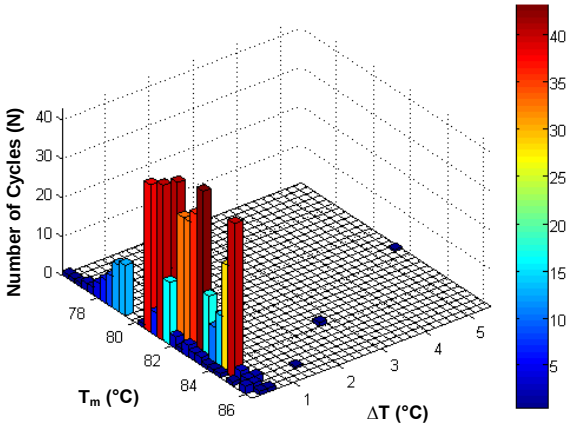


Figure 5.7 Rain flow thermal cycling data

The mean temperature changed between 76°C to 88 °C and highest cycle was observed as 40°C at 82°C mean temperature. In order to calculate the total lifetime consumption caused by the variable wind speed operation, Palmgren-Miner linear damage accumulation rule [254] was applied and modelled for failure prediction. The total life consumption results can be depicted in Figure 5.8. TLC for one wire bond of the inverter was found as 1.88 x 10^{-5}, and it was observed that the higher speed caused more life consumption for the inverter.

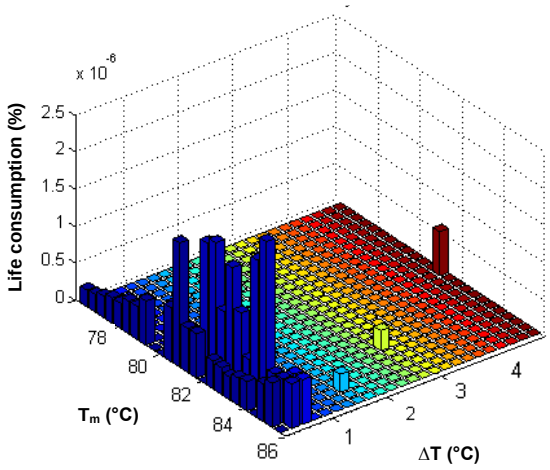


Figure 5.8 Lifetime Consumption during variable speed

It can be seen from the Figure 5.8 that, during wind speed increment, the mean temperature inclines and the number of cycles found in the thermal profile are increases. This causes more lifetime consumption for the device and decreases its reliability.

5.3 Lifetime Analysis for Discrete IGBT Devices

Lifetime models available in literature were used in previous sections in order to find the total life consumption for the solder layers and wire bonds of the multichip power electronic modules. However, for discrete, single chip devices studied in Chapter 3, there is no any specific lifetime model. Therefore, a lifetime consumption study was performed in this section to extract the parameters for the discrete IGBT device. Based on the discussed models in literature [1]-[183], a scheme of the lifetime consumption study, performed in this research, is shown in Figure 5.9. This model will be further used for a case study to analyse lifetime consumption of PECs used in a PV system.

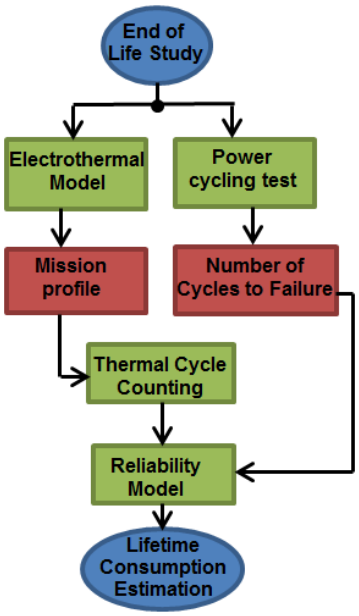


Figure 5.9 Scheme of lifetime consumption study

Initially, number of cycles to failure was obtained by an accelerated power cycling test. Implemented test circuit for reliability test can be seen in Figure 5.10. The gate signal duration was provided through dSPACE to turn on and off the device. Load current was conducted through power supply unit for generating temperature swing.

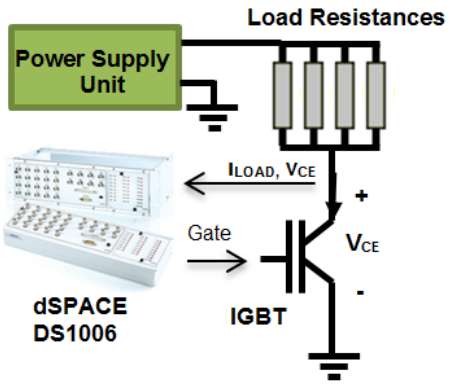
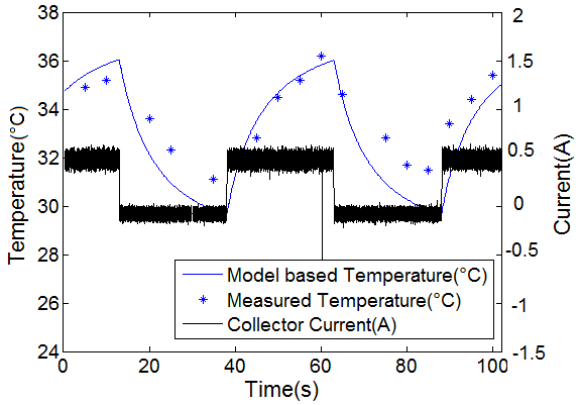
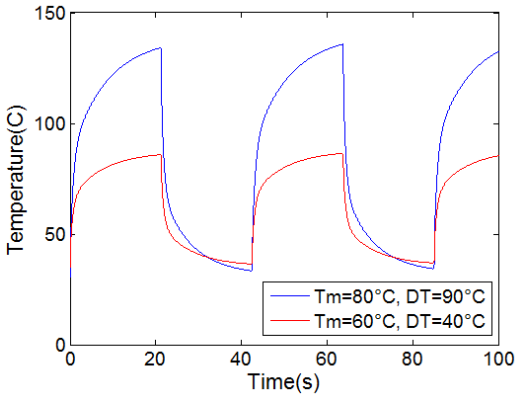


Figure 5.10 Accelerated life consumption test set-up

Modelled and measured temperatures are shown in Figure 5.11 (a) with respect to device current. A total of four different test conditions were applied for the failure test. Model based data is shown in Figure 5.11 (b) when the temperature swing (ΔT) was adjusted as 90°C and 40°C with average temperatures (T_m) of 80°C and 60°C, respectively.



(a)



(b)

Figure 5.11 (a) Temperature monitoring verification by thermal camera (b) Accelerated power cycling test data

The thermal resistance increment is common since the solder fatigue and the on-state voltage increment is caused by the wire bond lift off [17]. Hence, device temperature and the forward voltage of the IGBT were monitored during the test, as shown in Figure 5.12. The mean temperature was 60°C and temperature variation was 90 °C.

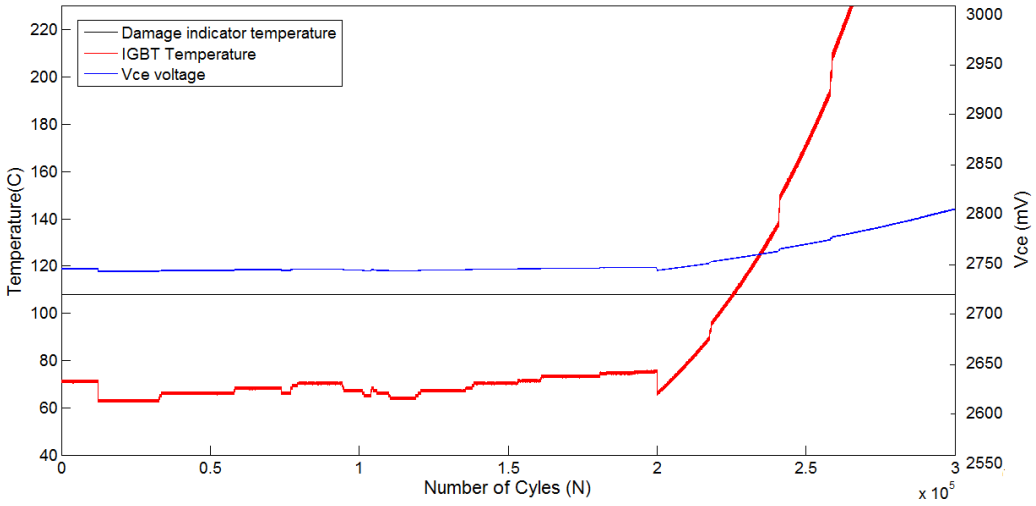


Figure 5.12 Power Cycling Test Results

Failure criteria were defined as 25% increase of temperature. Voltage across the device was no longer constant after 190k cycles and more than 30% increase was detected in the device temperature after 225k cycles. This was considered as indication of failure. A modified Coffin-Manson-Arrhenius lifetime model [183] was used to define cycle to failure data as a function of mean temperature, T_m and temperature variation ΔT. In the model, N_f is expected number of cycles to failure, Boltzman constant (k_b) is 1.38 x 10^{-23} J·K–1, activation energy is 1.3 x 10^{-19} J, A and α are the constants, 610 and -5, respectively which are fitted by least square method. Lifetime curves are presented in Figure 5.13 as a function of temperature variation with respect to number of cycles to failure.

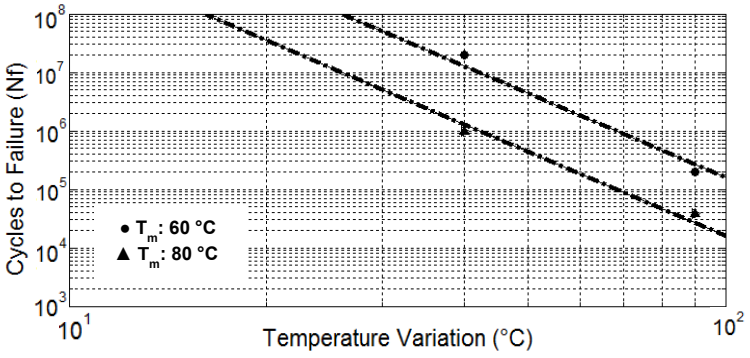


Figure 5.13 Lifetime curves

For lifetime estimation analysis purpose, Rainflow counting algorithm tool [256] was used to evaluate the temperature variation profile for the IGBT when P&O and IC MPPT algorithms were applied to PV system in the following section.

5.4 Case Study: Lifetime Analysis for PECs used in Solar PV Applications

Solar photovoltaics (PVs) have nonlinear voltage-current characteristics, with a distinctive maximum power point (MPP) depending on the environmental factors, i.e. temperature and irradiance. To harvest the maximum available power from the solar panels, maximum power point tracking (MPPT) techniques are used. In this section the effect of MPPT techniques on the lifetime of the PECs will be analysed. The most commonly used techniques namely Perturb & Observe (P&O) and Incremental Conductance (IC) methods were selected for this purpose. The PV solar cell internal photocurrent, I_{PH}, within PV cell equivalent circuit is shown in Figure 5.14 along with the boost converter for MPPT application purpose.

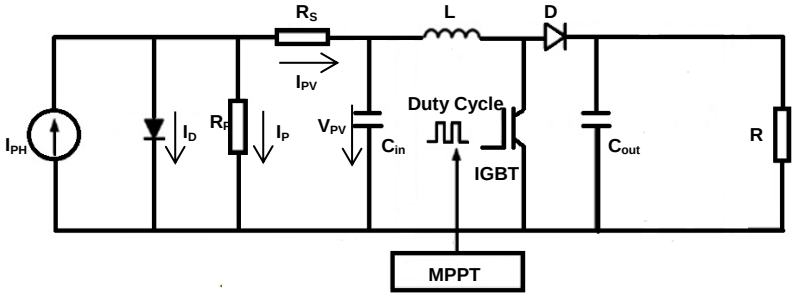


Figure 5.14 PV solar cell equivalent circuit integrated within a MPPT system

A parallel diode, *D*, internal series and parallel resistances (R_S and R_P) can also be seen in this circuit along with total current and voltage I_{PV} and V_{PV}, respectively. Total current, I_{PV}, can be represented with respect to diode, I_D and parallel resistance currents, I_P as:

$$I_{PV} = I_{PH} - I_D - I_P \tag{5.9}$$

$$I_{PV} = I_{PH} - I_0(\exp[\frac{q(V_{PV} + I_{PV}R_S)}{AkT_c}] - 1) - \frac{V_{PV} + I_{PV}R_S}{R_P} \tag{5.10}$$

where I_0 is the total diffusion current, V_{PV} is the output voltage, q is the charge of one electron, T_c is the solar cell temperature, k is the Boltzmann constant and A is junction perfection factor, which determines the diode deviation from the ideal p-n junction. For deriving the numerical model of a PV module, eqn. 5.10 can be extended as:

$$I_{PV}(1+\frac{R_{sT}}{R_{shT}}) = n_p I_g - n_p I_0(\exp[\frac{q(\frac{V_{PV}}{n_s}+I_{PV}R_{ST})}{AkT_c}]-1) - \frac{V_{PV}/n_s}{R_{shT}} \quad (5.11)$$

where I_g is photo-generated current, n_p cells in parallel and n_s cells in series the $R_{shT} = \frac{n_p}{n_s} \times R_P$ and $R_{sT} = \frac{n_s}{n_p} \times R_s$. PV voltage, V_{PV} as a function of the current, I_{PV} is represented [209] as:

$$V_{PV} = 2n(kT_c/q)n_s \ln(\frac{n_p I_g - I_{PV}}{n_p I_0}+1) - \frac{2n_s R_s}{n_p} I_{PV} \quad (5.12)$$

A PV module, namely KS10T by SOLARTEC, was used in this research due to its convenient power characteristics with the previously implemented DC/DC boost converters. The characteristic of the PV module used in this work is listed in Table 5.1. Based on eqn. 5.9-5.12, electrical model of this component was implemented by using MATLAB/Simulink.

Table 5.1: PV module parameter specifications

Electrical Performance (at 1kW/m^2)	Maximum Power	Maximum Power Voltage	Maximum Power Current	Open Circuit Voltage (V_{oc})	Short Circuit Current (I_{sc})
Values	54 W	17.4 V	3.11 A	21.7 V	3.31

5.4.1 Maximum Power Point Tracking (MPPT) Algorithms

P&O and IC algorithms were implemented for MPPT purpose in MATLAB/Simulink. The maximum power point, expression, $P_{PV,mpp}$, can be written as [208]:

$$P_{PV,mpp} = I_{PV,mpp}.V_{PV,mpp} = (I_{PH} - I_0\left[\exp(qV_{PV,mpp}/AkT_c)-1\right])V_{PV,mpp} \quad (5.13)$$

5.4.1.1 Incremental Conductance (IC) MPPT Algorithm

Incremental conductance (IC) MPPT method is based on the derivative of the power with respect to the voltage at P-V curve which is equivalent to zero at maximum power point. Hence, by comparing the instantaneous conductance (I_{pv}/V_{pv}) with incremental one ($\Delta I_{pv}/\Delta V_{pv}$) maximum power point is tracked based on the sign of the $\Delta P_{pv}/\Delta V_{pv}$ and varying the operating voltage. Flowchart of IC methods can be seen in Figure 5.15 (a).

$$\frac{dP_{pv}}{dV_{pv}} = \frac{d(V_{pv}I_{pv})}{dV_{pv}} = I_{pv}\frac{dV_{pv}}{dV_{pv}} + V_{pv}\frac{dI_{pv}}{dV_{pv}} = I_{pv} + V_{pv}\frac{dI_{pv}}{dV_{pv}} \cong I_{pv} + V_{pv}\frac{\Delta I_{pv}}{\Delta V_{pv}} \tag{5.14}$$

The maximum power point of solar PV module can be defined as:

$$\frac{dP_{pv}}{dV_{pv}} = 0 \Rightarrow I_{pv} + V_{pv}\frac{dI_{pv}}{dV_{pv}} = 0 \Rightarrow -\frac{I_{pv}}{V_{pv}} = \frac{dI_{pv}}{dV_{pv}} \tag{5.15}$$

from eqn. 5.15, operating points of the PV module with respect to IC algorithm can be written as:

$$\frac{dP_{pv}}{dV_{pv}} = 0, \; for \;\; V_{pv} = V_{pv,mpp} \;\; and \;\; \Delta I_{pv}/\Delta V_{pv} = -I_{pv}/V_{pv} \tag{5.16}$$

where the module is operated at MPP and the V_{pv} should be hold as it is.

$$\frac{dP_{pv}}{dV_{pv}} > 0, \; for \;\; V_{pv} < V_{pv,mpp} \;\; and \;\; \Delta I_{pv}/\Delta V_{pv} > -I_{pv}/V_{pv} \tag{5.17}$$

where the V_{pv} should be increased by applying constant steps to reach $V_{pv,mpp}$.

$$\frac{dP_{pv}}{dV_{pv}} < 0, \; for \;\; V_{pv} > V_{pv,mpp} \;\; and \;\; \Delta I_{pv}/\Delta V_{pv} < -I_{pv}/V_{pv} \tag{5.18}$$

where the V_{pv} should be controlled by applying constant steps to be reduced until $V_{pv,mpp}$.

5.4.1.2 Perturb & Observe (P&O) MPPT Algorithm

Perturb & Observe (P&O) MPPT algorithm is derived by producing disturbances to either instantaneous current or voltage which was used as a reference in this study. By changing the solar panel voltage in small amounts, the system I-V operating point and hence P-V characteristics are changed. However, change in amount of power can either be positive or negative. In case that it is positive; disturbance should follow the same direction until MPP is approached. Otherwise, perturbation direction should be changed to prevent moving further away from MPP. Step size of the disturbance can be decreased when it is closer to MPP to avoid large oscillations. Flowcharts of P&O method is shown in Figure 5.15 (b).

5.4.2 Electro Thermal Model of Boost Converter within MPPT

A Boost DC/DC converter with NPT IGBT device, implemented in Chapter 3, was used for matching the MPP of the PV module at any irradiance and temperature level along with an MPPT control, PWM block and a load. Operating point of the PV module is changed by the duty cycle of the switching element (IGBT) according to MPPT algorithms to reach the single value of maximum power point duty cycle, D_{MPP}. By recalling the boost converter topology, operating occurs in ON and OFF stages in period of T. During ON stage, for DT seconds, the IGBT is closed which results in increase of the inductor current. During the flow through the IGBT, power losses occur on this device due to drastic change in current and voltage; hence, its temperature increases. Thermal cycling on this component results in deformation and eventual failures which is around 60% of overall PEC runaways.

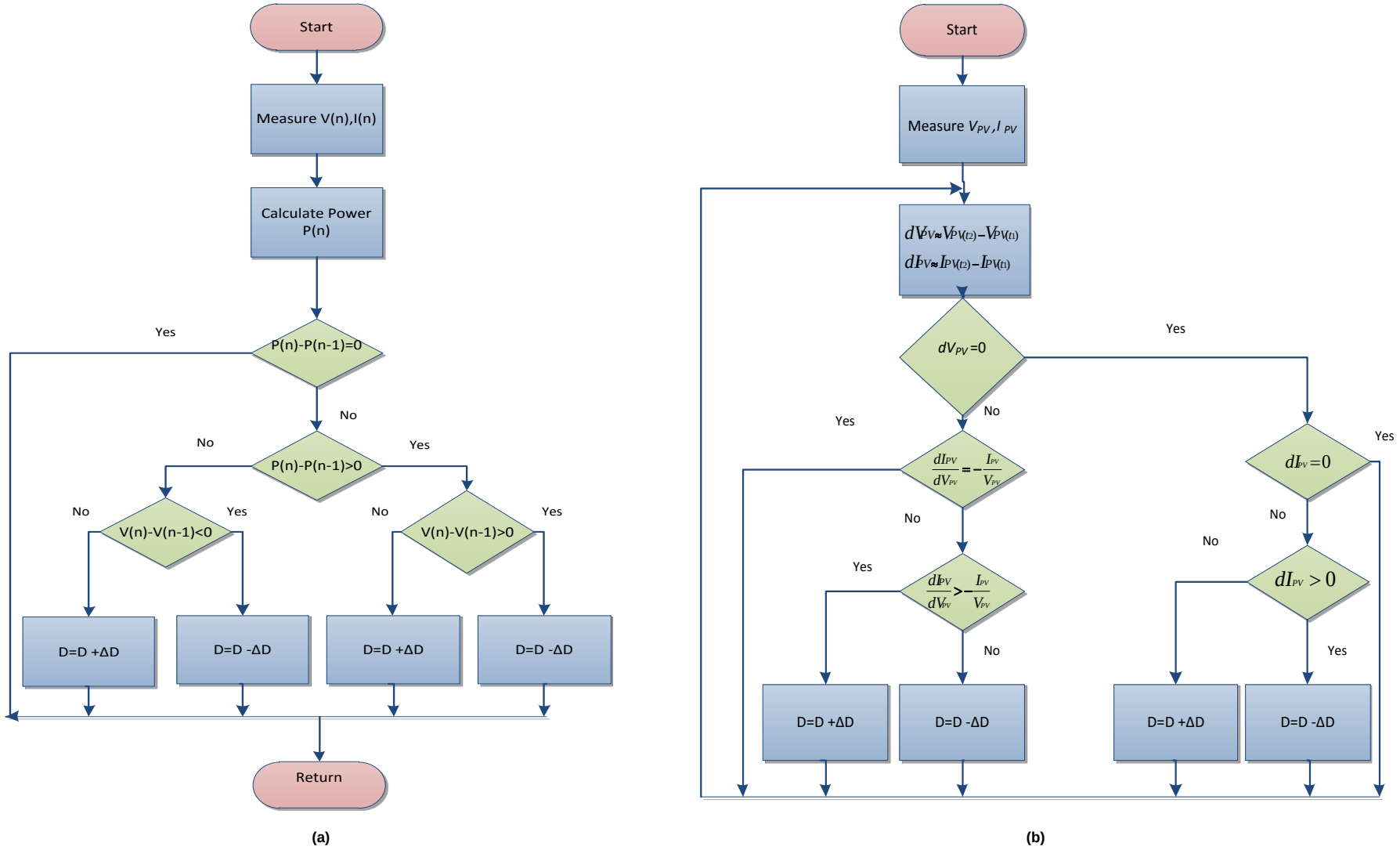


Figure 5.15 Flowchart of (a) Incremental Conductance and (b) Perturb & Observe Methods

Therefore, only electro thermal model of this device was implemented. When IGBT is open, for *(1-D)T* seconds, energy accumulated into the capacitor and load through flyback diode. At this stage, no heat losses occur. For both stages, circuit equivalences of the converter, when coupled with PV module, can be written as:

$$\frac{V_{PV}}{L} t_{on} = -\frac{V_{PV} - V_{OUT}}{L} t_{off} \tag{5.19}$$

$$\frac{V_{PV}}{L} DT = -\frac{V_{PV} - V_{OUT}}{L} (1-D)T \tag{5.20}$$

eqns. 5.19 & 5.20 can be simplified into the relationship between input /output voltage as:

$$\frac{V_{PV}}{V_{OUT}} = 1 - D \tag{5.21}$$

5.4.3 Experimental Setup

MPPT algorithms were individually implemented using Simulink and integrated with dSPACE through control desk. Gate signals generated through MPPT blocks were provided through DS5101 digital to analogue converter card. Due to gate requirements, gate drivers were used to reach sufficient power level. Experimental setup is shown in Figure 5.16.

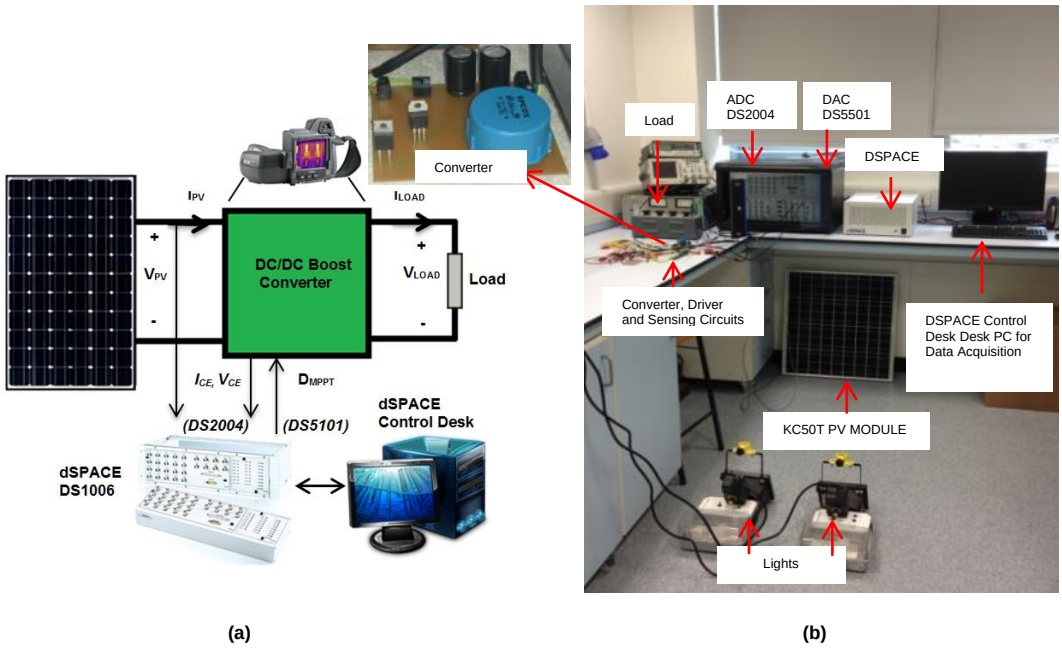
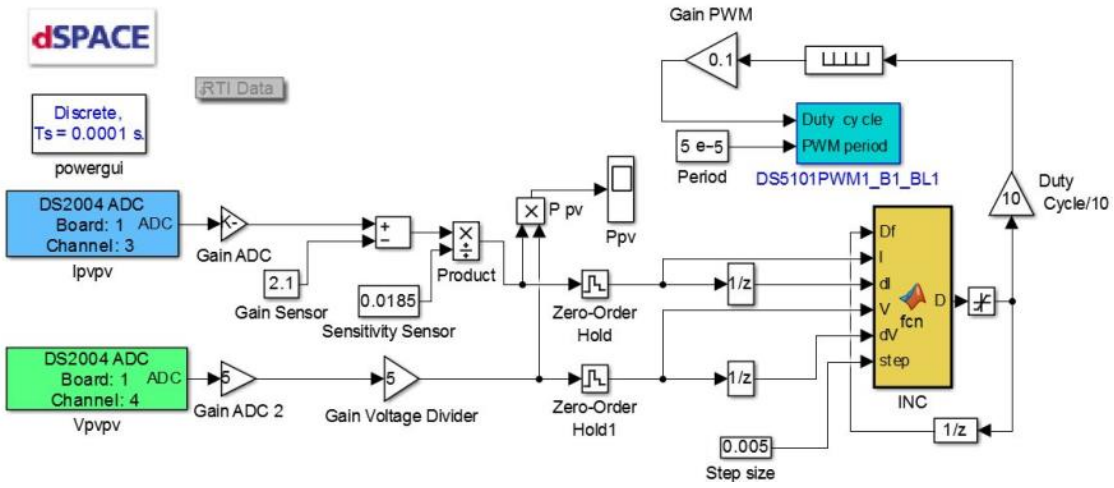
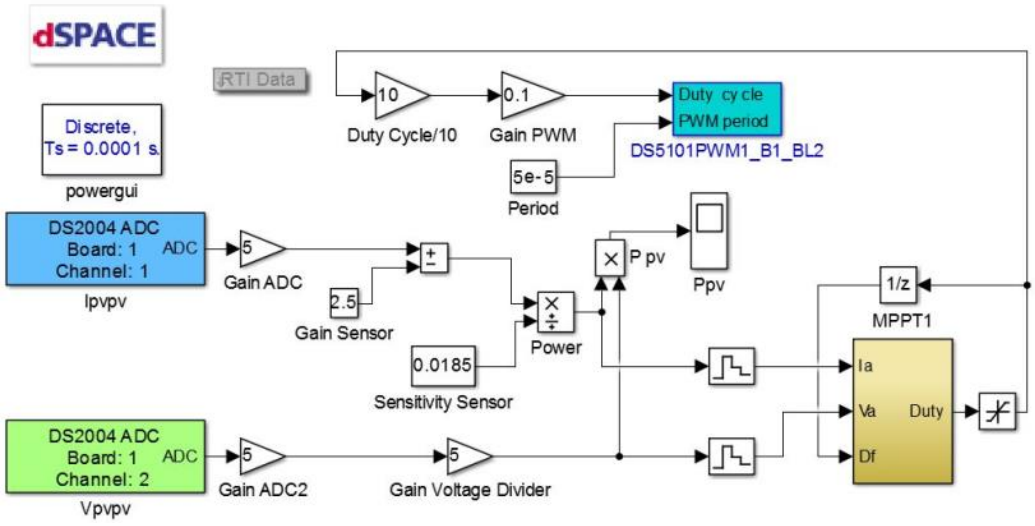


Figure 5.16 (a)Visual and and (b) Actual cxperimental Set-up

Collector current, I_{ce}, and PV current, $I_{PV,}$ were monitored by current transducers, LA 25-NP, and were inserted dSPACE RTI through DS2004ADC as power loss and MPPT algorithm model inputs. PV and collector to emitter voltages, V_{PV} and V_{ce} were also measured for operating within same blocks as current signals. Implemented IC and P&O algorithms within Simulink and dSPACE are shown in Figure 5.17 (a) & (b), respectively.



(a)



(b)

Figure 5.17 Real Time Implementation of (a) IC and (b) P&O MPPT methods in dSPACE

Look up tables were used to interpolate previously estimated switching energy loss profiles during switching operation. Real time power loss profiles were monitored by multiplication of these losses with the switching frequency. Then, total power loss was calculated over one switching period in each step time as a function of collector current, I_{ce}, collector to emitter voltage V_{ce} and temperature by addition of switching and conduction losses.

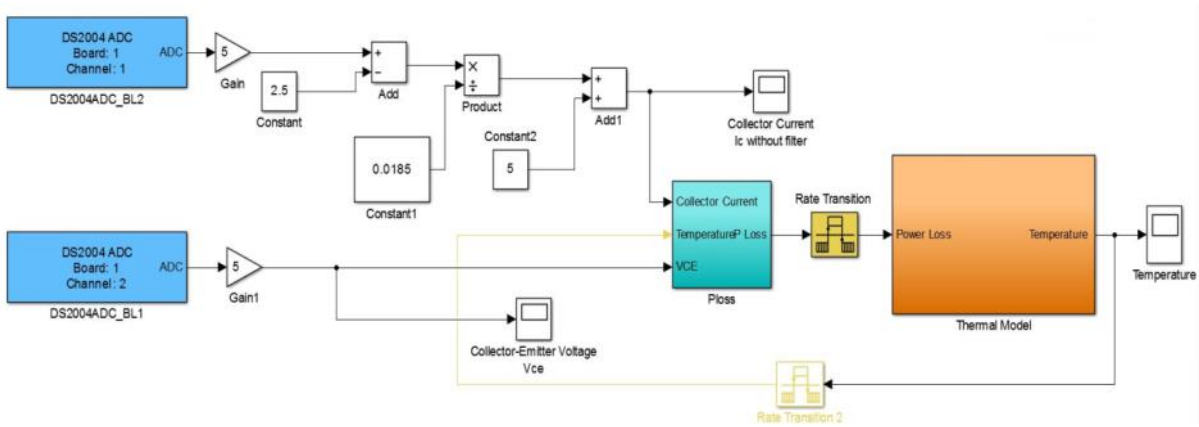


Figure 5.18 RT Implementation of Electro thermal Model in dSPACE

Total power losses were then used as input to heat source within thermal model, as shown in Figure 5.18 by using Simulink blocks, as already studied in Chapter 3, mathematical equivalent model was implemented in thermal block. Estimated temperature is then fed back into power loss model for continuous monitoring.

5.4.4 Electro Thermal performance of PEC with IC and P&O methods

5.4.4.1 Simulated and Experimental Characteristics of PV Module

PV module performance was examined under different light irradiation levels experimentally and compared with numerical simulation results. MATLAB s-functions were used to execute the PV voltage/current characteristic by coding. The boost converter model in Simulink was then embedded to the PV system model which provides the input power. I-V and P-V characteristics under different irradiation levels are shown in Figure 5.19 (a) & (b) when different load characteristics were applied experimentally along with numerical simulation which results at 22°C ambient temperature.

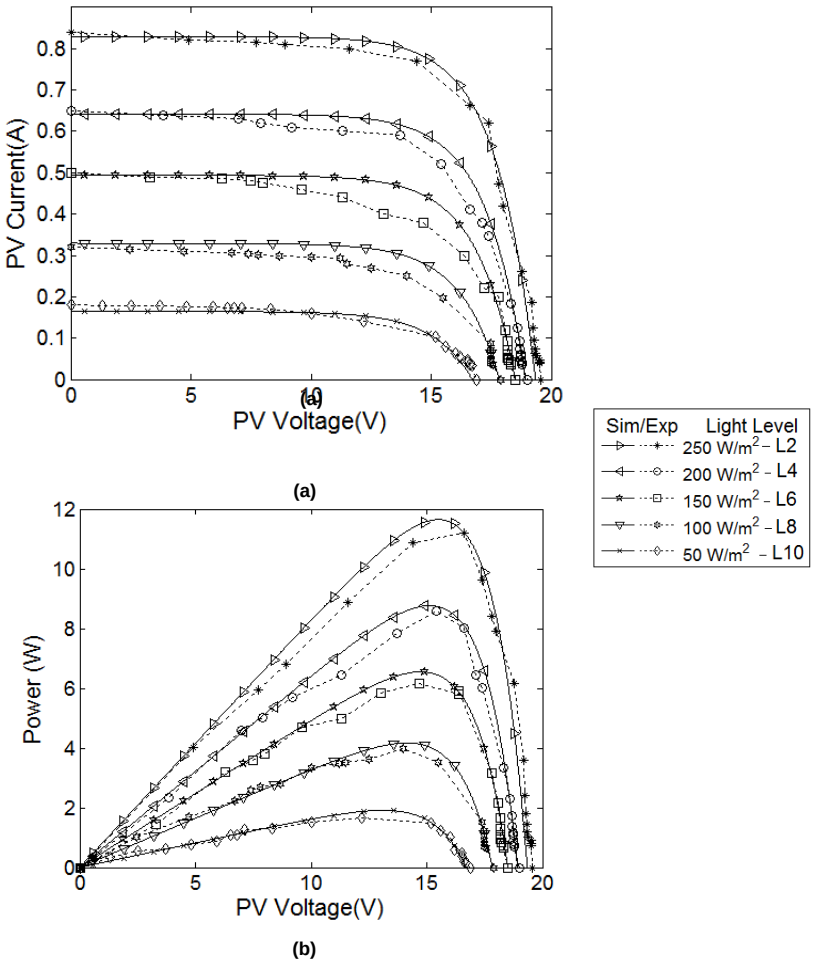
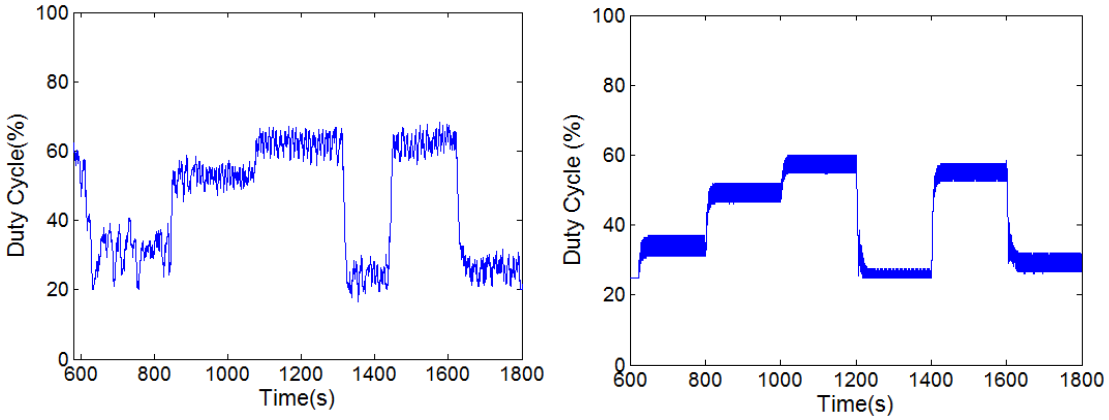


Figure 5.19 Experimental a) I-V and b) P-V characteristics at different light levels of halogen bulb

In order to assess an accurate temperature monitoring with thermal camera, no heat sink was attached to switching device. Light controlled chamber, with ten portions, was used to vary irradiance. By this way, any thermal runaway on PECs was avoided due to the increased current characteristics at higher light level. As light level decreases, MPPT voltage changes more drastically compared to higher light level. Hence, wider ranges of duty cycle operating points were examined for verifying thermal stress difference between P&O and IC algorithms.

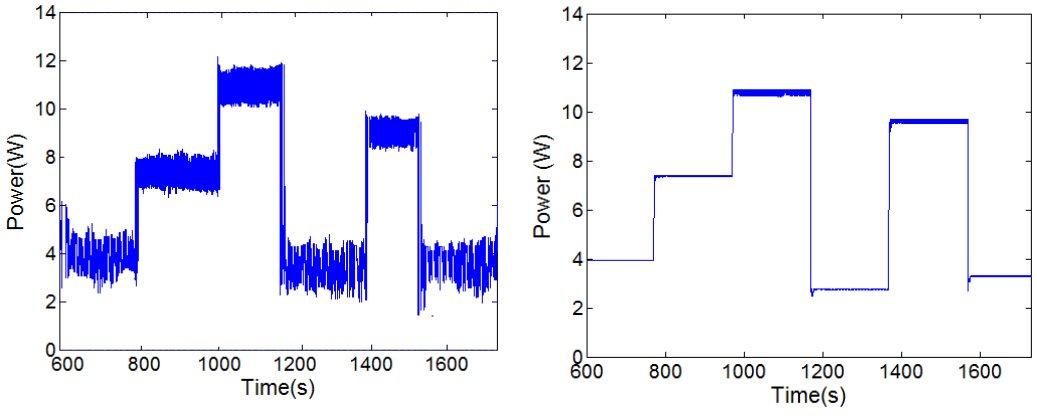
5.4.4.2 Electro Thermal Comparison of IC and P&O MPPT Algorithms

Thermal performance of IC and P&O methods was tested under the same environmental conditions. Experimental and simulated PV voltages, current and tracked maximum power as well as the length of the duty cycle by means of percentage are shown in Figures 6.20-6.23 (a) and (b), respectively for IC algorithm based MPPT.



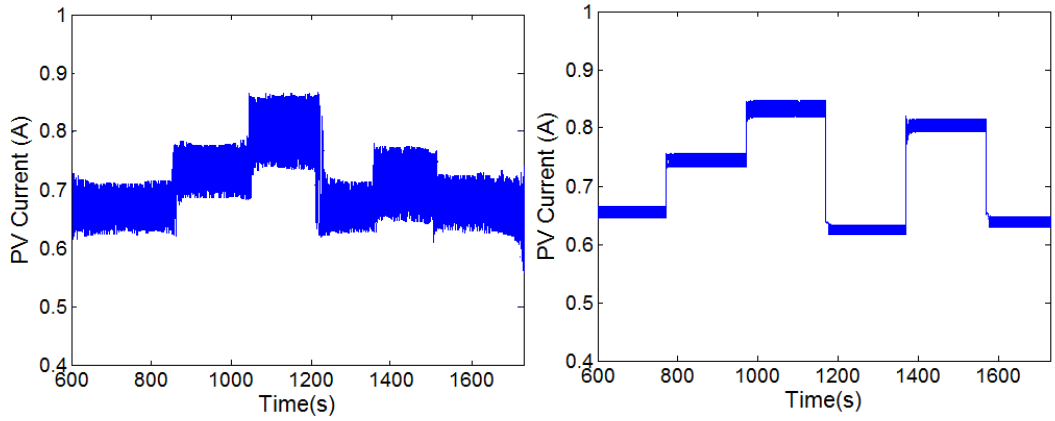
(a) (b)

Figure 5.20 (a) Experimental and b) Simulated MPPT duty cycle with IC method



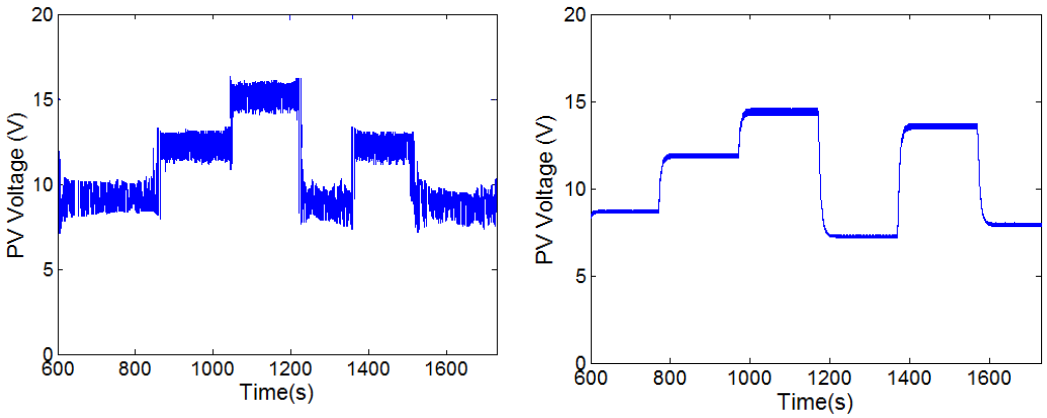
(a) (b)

Figure 5.21 (a) Experimental and (b) Simulated MPPT power with IC method



(a) (b)

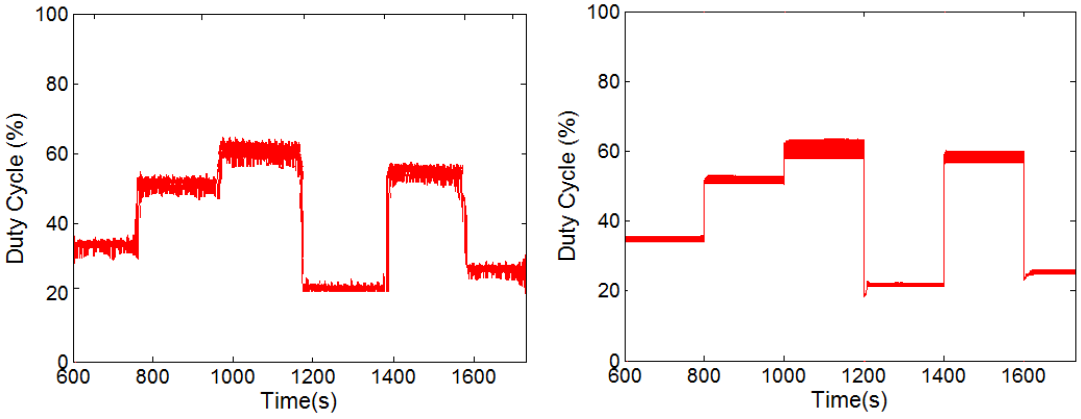
Figure 5.22 (a) Experimental and (b) Simulated MPPT current with IC method



(a) (b)

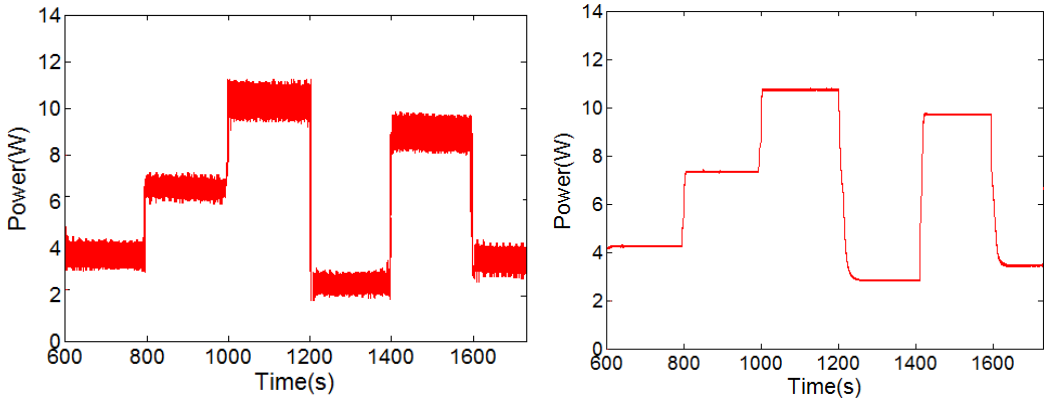
Figure 5.23 (a) Experimental and (b) Simulated MPPT voltage with IC method

The analysis can be seen in Figures 5.24-5.27 when the MPPT method P&O was used. Duty cycle changes during operation in IC algorithm are more drastic compared to the P&O algorithm as it can be illustrated in Figures 5.20-5.27. The gradual change of duty cycle in P&O algorithm was also reflected on the extracted PV current characteristic. Although, it is more oscillatory, the amplitude during each cycle is less compared to the IC method. In general, both methods show inaccuracies at low light levels where P&O provided slower response to light level changes during all practical and experimental analysis.



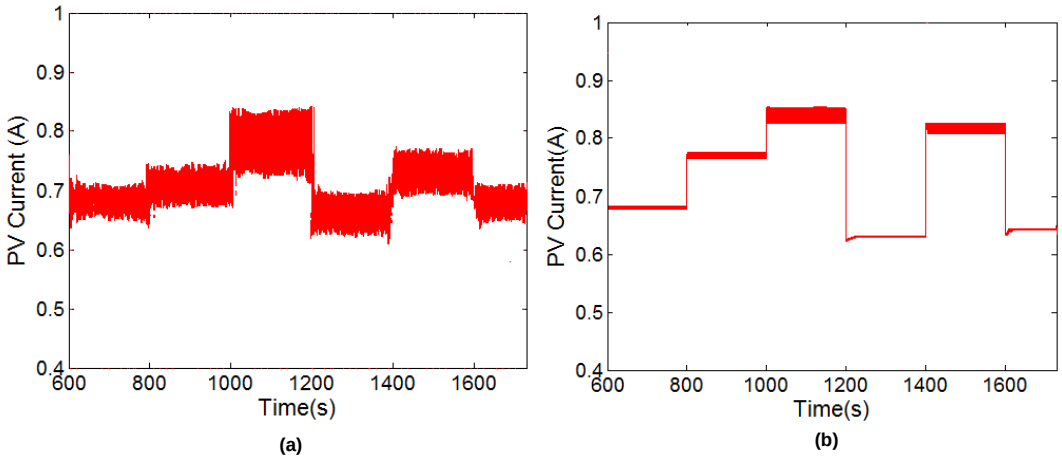
(a) (b)

Figure 5.24 (a) Experimental and (b) Simulated MPPT duty cycle with P&O method



(a) (b)

Figure 5.25 (a) Experimental and (b) Simulated MPPT power with P&O method



(a) (b)

Figure 5.26 (a) Experimental and (b) Simulated MPPT current with P&O method

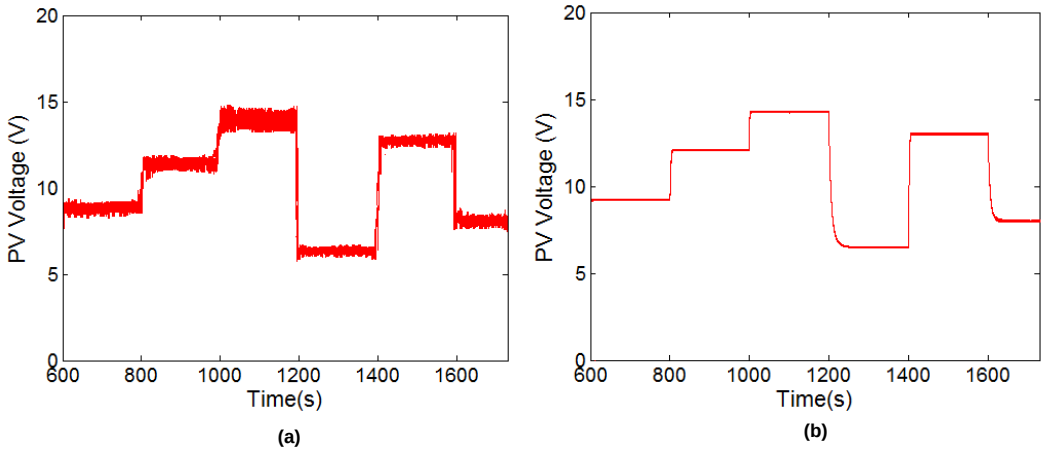


Figure 5.27 (a) Experimental and (b) Simulated MPPT voltage with P&O method

Power loss profiles of semiconductor switching devices are highly depended on the current signal characteristic i.e. amplitude, frequency etc. [104], [233], [257]. This was monitored on dSPACE Control Desk for both MPPT methods, as illustrated in Figure 5.28 (a). It can be clearly seen that there is higher power loss profile especially when higher illuminations between 1000 and 1200 & 1400 and1600 seconds are experienced for IC method. The gradual current change caused more fractional loss profile when P&O was selected as MPPT method and approximately 10 W less power loss can be attained compared to IC one at highest possible light level.

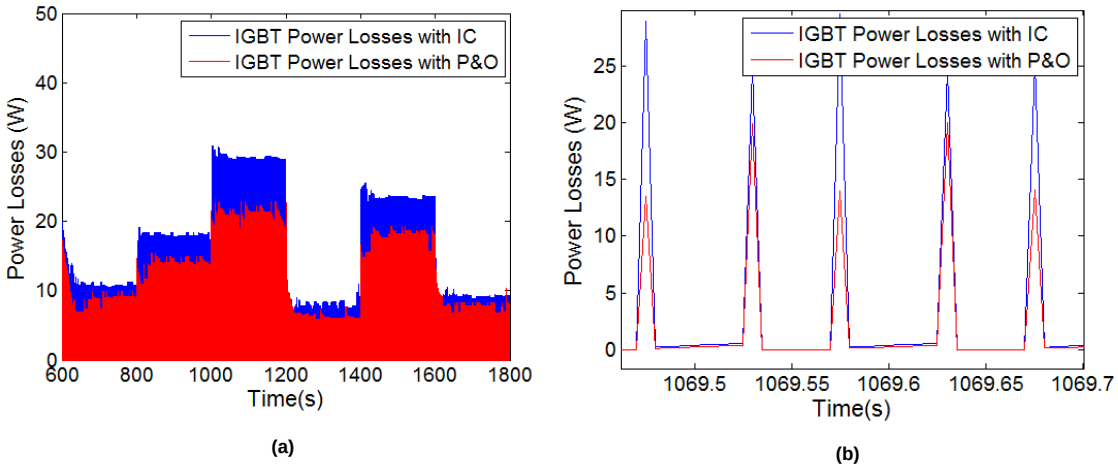
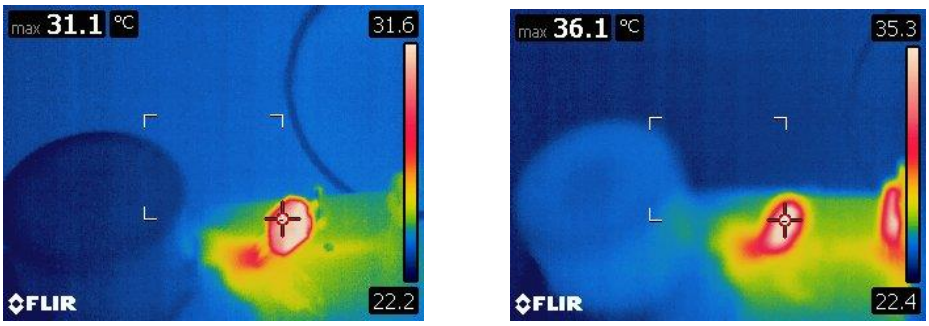


Figure 5.28 (a) Total power loss and (b) switching losses comparison on IGBT when IC and P&O selected

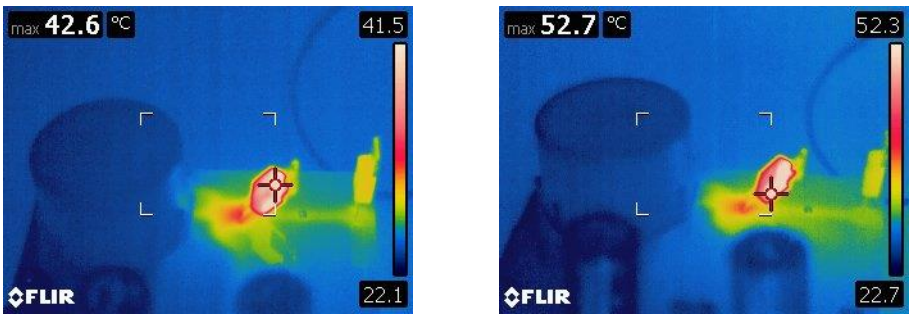
Switching energy losses for a fraction of analysis time are depicted in Figure 5.28 (b). The sharp change of PV current caused by tracking method which is the result of light level change, produced more switching losses when IC algorithm is selected. Approximately, two and half times higher power loss can be noticed during on-time losses where the device is exposed the highest voltage/current change. Yet, off-time losses were very similar in both methods.



(a) (b)

Figure 5.29 Thermal camera view of IGBT when the light level is 6 (4150 Lux) when (a) P&O and (b) IC used

Temperature of the PEC was monitored by FLIR T440 thermal camera [258]. Tests were performed under 22°C ambient temperature. Thermal impedance values in thermal model were also verified by this method. Thermal camera captures for temperature difference observation when P&O and IC methods were used under light level 6 and 10, are shown Figures 5.29 and 5.30, respectively.



(a) (b)

Figure 5.30 Thermal camera view of IGBT when the light level is 10 when (a)P&O and (b)IC used

Operating temperature of IGBT is the highest compared to other components' located on PEC. Nevertheless, the IGBT experienced approximately 10 °C higher temperature when the IC method is selected with 52.7 °C compared to 42.6 °C with P&O highest light level, as

shown in Figure 5.30. Therefore, higher power loss profile caused by IC method affected the operating temperature of the IGBT, proportionally. Transient experimental temperature characteristic of the IGBT can be seen in Figure 5.31 (a) which was observed through in dSPACE Real Time Control Desk where Figure 5.31 (b) shows the simulated results in Simulink.

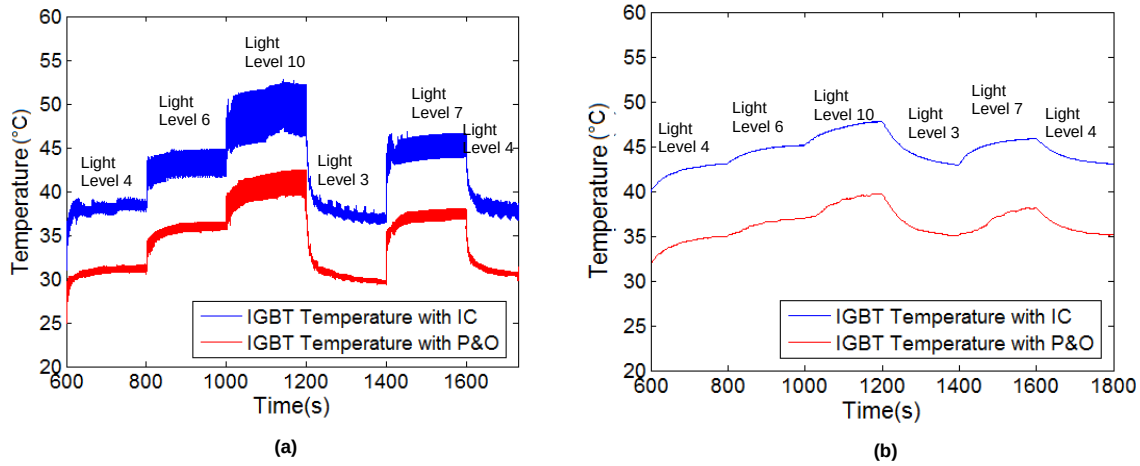


Figure 5.31 (a) Transient IGBT temperature monitored in dSPACE, (b) Simulated temperature in Simulink

Steady state temperatures of IGBT captured by thermal camera for each applied light level can also be illustrated in Figure 5.32.

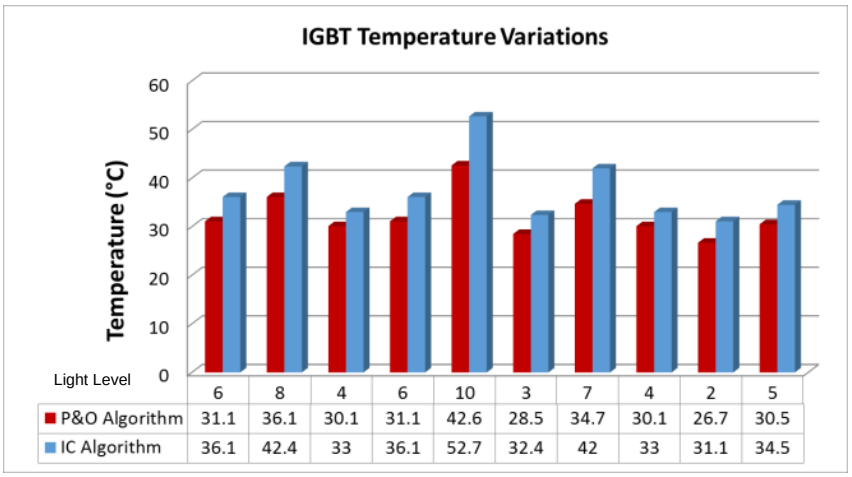


Figure 5.32 Steady state IGBT temperature comparisons when IC and P&O selected as MPPT methods

As it can be depicted, a very good approximation was obtained at specified light levels on the PV module with the modelling method. Meanwhile, the IGBT temperature amplitude difference between P&O and IC methods inclines as the light level; hence, the MPP

increases. Approximately 6 °C temperature cycling is observed at the light level 10 when IC was used with up and down boundaries of 52 and 46 °C, respectively. Yet, with P&O based system, the fluctuations are as low as 4 °C from 42 to 38 °C, although temperature amplitude changes more drastically along with light level variations.

5.4.4.3 Lifetime Modelling and Reliability Comparison of IC and P&O MPPT Algorithms

Temperature profiles obtained in Figure 5.31 (a) was processed in the Rainflow counting algorithm. The counted numbers of cycles for both temperature profiles are shown in Figure 5.33 (a) & (b). The majority of thermal variations (ΔT) are estimated at low values for both algorithms and the mean temperature changes (Tm) between 40 °C -55 °C for IC and 35 °C - 45 °C for P&O. The highest number of cycles for IC is approximately 2000 at 43 °C where it is 2500 cycles for P&O algorithm at 35 °C.

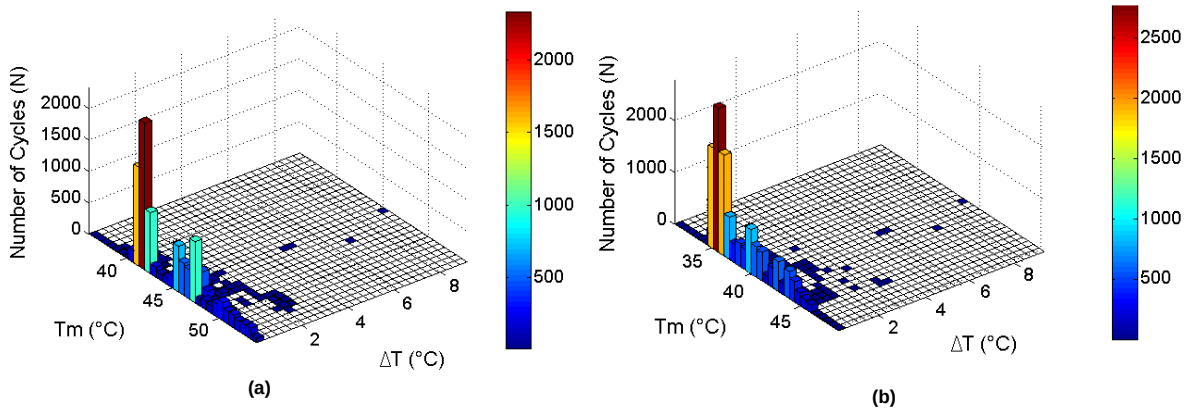


Figure 5.33 Number of cycles found with (a) IC and (b) P&O algorithms

Numbers of life consumption of IGBT for IC and P&O algorithms are shown in Figures 5.34 (a) & (b). The TLC was calculated by addition of each consumption data by using the model experimentally implemented in Section 5.3. As it can be observed, less amount of high temperature variation i.e. at 10 °C mean temperature of 43 °C for IC and 35 °C for P&O methods cause approximately same amount of life consumption with ten times higher number of cycles at low temperature variation (i.e. 0.5 °C) at 5 °C higher mean temperatures. TLC for IGBT, used in boost converter, was found as 4.817 x 10-5 while this was 3.44 x 10-5 for P&O algorithm. Thus, approximately 1.4 times higher TLC was observed

for the IC MPPT method usage under same loading and environmental conditions compared to the P&O algorithm for the described PV system.

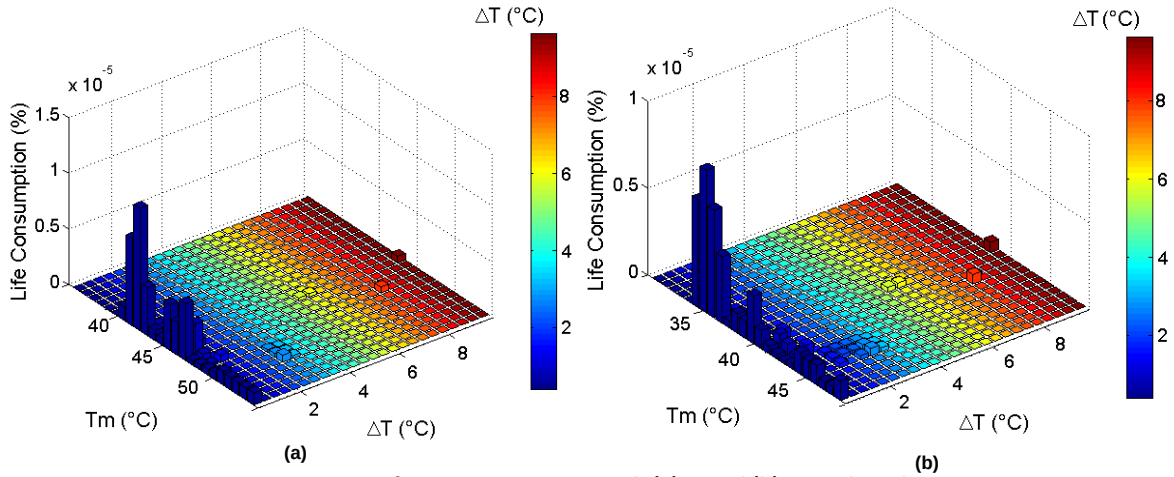


Figure 5.34 Lifetime Consumption with (a) IC and (b) P&O algorithms

5.4.5. Discussion

Prior to discuss the reasons behind the different temperature profiles of the switching device of the converters while operated by P&O and IC MPPT algorithms, it is worth to recall their operating principles and main causes of the electro thermal power loss occurring which affects the reliability.

The P&O algorithm simply introduces perturbations in the duty cycle of the power converter which leads to changes in the PV voltage and current. Subsequently, by observing the change in the operating power, the duty cycle is further increased or decreased by the amount of the perturbation step size as the direction of the perturbation is retained. It should be noted that, once the maximum power point is reached, the conventional P&O algorithm begins to oscillate around it by a certain amount, depending on this perturbation step size.

The IC, on the other hand, incrementally compares the ratio of the derivative of the conductance with the instantaneous conductance and updates the duty cycle, accordingly. Similar to the P&O, the maximum power point where the condition of dI/dV + I/V = 0 is difficult to be operated; hence the PWM signal oscillates around this point.

Although in theory, both methods provide very close tracking efficiencies as discussed in literature, the working principle of the P&O consists of a hill climbing nature which has

slower dynamics compared to the IC algorithm's incremental ratio working principle. This is the one main reason for the difference in the average values of the tracking efficiencies between both algorithms where the INC performs 3% better for the applied test conditions compared to the P&O. The selected perturbation step time, which is 0.005, has also a significant effect on the efficiency and oscillations during varying irradiance conditions. A further optimised perturbation step size would increase the efficiency for both methods and vice versa.

The efficiency of the P&O method is low at the sharp decrements of the light levels such as at 600, 1200 and 1800 seconds due to the constant perturbation size. The same method has better efficiency at the higher light levels; however it is not as high as the IC due to its slower dynamics. One other reason is that the perturbation step is not sufficient to follow rapid increase in the MPP. Yet, the IC has faster working dynamics and provides better tracking efficiency under minimum and maximum light conditions. It continuously inspects the ratio between derivative and instantaneous conductance to update the duty cycle rather than producing perturbations and updating the duty cycle based on the direction of the slope by using a hill climbing method. The searching direction can get confused with P&O due to experimental noise which results in reduced tracking efficiency as well. On the other hand, at medium light levels, i.e. 5-7, the efficiency between both algorithms was found similar.

Lower efficiencies at low light level conditions, i.e. around 1-3, are due to the constant perturbation step size which causes undesired oscillations on the very low current drawn from the PV panel. The current oscillations result in oscillations in power and the MPP tracking is affected negatively for both P&O and INC methods. Specifically, the low efficiencies for the IC method at low light conditions are mostly related to the oscillatory behaviour of the duty cycle of the converter which does not allow the voltage and current to settle down smoothly as seen through Figures 6.20-6.23 (a) and (b); hence, the MPP condition cannot be stabilised constantly as mentioned in literature [218].

According to the experimental and simulated analysis discussed above, the IC method was found as more efficient compared to the P&O method under identical operating conditions which is in agreement with the previous literature studies. Specifically, the IC yield better efficiency for drastic light level changes and the P&O method has slower dynamics and

offers lower efficiency due to the perturbed PV output parameters (oscillation may cause divergence) in every MPPT cycle, although it is mostly accepted as easier to implement.
Having studied the tracking efficiency, the reflection of the dynamics of both methods on the electro thermal performance of the switching devices of the converters can be further analysed. To begin with, since the IC method was found as more efficient than the P&O method, theoretically it can deliver more power from the PV panel under identical working environment. This, in turn, results in more current drawn through the converter as experimentally and theoretically shown in Figures 6.20-6.27. It was initially stated that the current increase causes more power losses for the switching devices and it is also a function of both duty cycle and temperature. This is the main reason for the IC method why it has higher loss profile compared to the P&O method which causes higher temperature and life time consumption. In particular, for instance, at the highest light level, the duty cycle is increased by both algorithms to extract the maximum available power where the IC method showed better efficiency. The converter extracted 11.2 W average power once it is operated by IC whereas this was 10.5 W with the P&O method. The average duty cycle provided by the IC was 63% where it was only 59% from the P&O method. This clearly shows that with the IC method, longer conduction time occurred on the switching device compared to the P&O method. This leads to more current passing through the device in on-stage; hence, causes higher conduction losses as shown in Figures 5.28 (a) & (b). The increments in the average temperature profile with IC and the fluctuations are related to this analysis as can be depicted in Figures 5.31 (a) & (b). As a result of the lower temperature profile, the P&O caused 1.4 times less life time consumption on the switching device compared to the IC method.

5.5 Summary

Lifetime modelling for the PECs was completed in this chapter. Lifetime of such semiconductor component depends on the thermal variation caused by changing operating conditions. This was investigated in this work with experimental power cycling test based life time consumption monitoring. Number of cycles to failure was estimated by this test and number of cycles in temperature profile of IGBT used in PEC was counted by Rainflow

algorithm. Then, life time consumption was calculated based on the Palmgren-Miner linear damage accumulation rule. Based on this methodology, the total cycles to failure for the proposed variable DC-link switching frequency control method was calculated as 3.26×10^{-5} which is approximately 1×10^{-5} less consumption compared to the other both methods. The thermal stress analyses, obtained in Chapter 4, are also in good agreement with the related TLC results. The highest average stress occurred for the fixed DC-link operation which caused higher TLC and vice versa for the proposed switching frequency control method.

Effects of IC and P&O maximum power point tracking algorithms on the electro thermal performance and lifetime of the IGBT used as switching element of PEC were presented. Compared to the P&O method, thermal cycling on the IGBT component was found as approximately 4°C higher when the IC method is operated and the steady state temperature was 52.7°C while this was 42.6 °C with P&O. The system operated by IC method was found to be less reliable compared to the one with P&O, once they are operated under the same operating conditions. IC method was found to cause 1.4 more life consumption. Consequently, the IC method is superior in terms of tracking efficiency and response to sudden light level changes on PV module based on this study; however, it causes higher varied temperatures on IGBT and reduces its reliability. The results presented in research, for the first time in literature, clearly show that the reliability of the converter switching devices is affected by different MPPT methods in PV applications. An interesting future research needs to be done for further investigating of this phenomenon under different operating parameters i.e. power rating and environmental conditions.

Chapter 6

Achievements, Conclusions & Future Work

6.1 Overview

This chapter states the outcomes of the research project. Achievements and objectives are addressed and summarised by an overall conclusion of the proposed real time electro thermal modelling and experimental studies. Future prospects of the research work are also presented as future research directions.

6.2 Reviews for the Objectives and Achievements

The objectives of this research were fulfilled as follows:

Objective 1: To review the research status in the electro thermal modelling, operating conditions, physical material properties and reliability of insulated gate bipolar transistors operated in power electronic converters of renewable energy systems.

A comprehensive literature survey was presented in Chapter 2. Research status in electro thermal and thermo mechanical modelling of the power electronic converters and the limitations of current modelling approaches were defined. By reviewing the above research works, the research questions for the project is outlined. Reliability of the power electronic devices was defined as one of the most significant factor which affect the overall lifetime of the renewable energy systems. However, only few publications appear in literature which concerns to decrease these stresses by optimising the power losses of PECs. To assess estimation of this phenomenon, an accurate electro thermal modelling technique was presented which is applicable to be coupled with renewable energy system PECs.

Objective 2: To derive accurate electro thermal and thermo mechanical FE models for the semiconductor switching and power electronic devices used in renewable energy systems.

An accurate electro thermal model for a multichip single IGBT power module was achieved in Chapter 3. The model was built by using COMSOL finite element package and the thermal characteristic was embedded in Simulink package based on the complex heat interactions

and coupling effect across chips located on the device. Analytical results also showed good agreement with the model.

Objective 3: To investigate electro thermal characteristics of topologically different semiconductor switching devices based on their physical and operational differences.

In order to verify accuracy of the proposed electro thermal model, performance of trench gate topologically different IGBT devices with a silicon carbide based MOSFET were presented in Chapter 3. Experimental studies were conducted in order to evaluate the models in wide range of operating condition such as ambient temperature or load variations. By real-time implementation of dSPACE model, an efficient temperature monitoring tool was produced and subsequently, modelling outcomes are verified by using those devices as switching elements in operational boost converters.

Objective 4: To derive thermo mechanical FE models for power electronic devices used in renewable energy systems.

The thermo mechanical study was completed by using FE analysis for power electronic converters used in renewable energy systems in Chapter 4. Thermal stress effect was defined as von-Mises and principal stresses and observed based on the temperature variations on each chip located on the devices and the layers underneath.

Objective 5: To derive reliability models for semiconductor switching devices as a function of electro thermal and thermo mechanical characteristic.

Rainflow algorithm was used to estimate the total number of cycles in each temperature profile and by using improved Coffin-Manson methods the number of cycles to failure was obtained. The total life consumption was then calculated by Palmgren–Miner rule. Experimental validation of model based implementation of a three phase inverter module was presented in Chapter 5. The switching frequency control method for extending lifetime of the associated inverter was verified by a physical variable speed wind turbine. The model is validated via dSPACE real time implementation with an actual permanent magnet

generator based wind turbine system test rigs. Further discussion was presented in order to verify the thermal stress analysis with total life time consumption calculations.

Objective 6: To implement Simulink models of wind and PV systems with embedded power electronic converters and their associated control algorithms to decrease the thermal stress and enhance the lifetime during variable environmental conditions.

In order to decrease thermal stress occurring on PECs, a switching pattern control method was derived in Chapter 4. During a variable wind speed application, the methods were able to decrease significant amount of stress which led to enhance the lifetime. The effects of maximum power point tracking algorithms on lifetime in DC-DC converters under different operating conditions was investigated for the first time in literature. Experimental work was verified in Chapter 5 by real time implementation of model based photovoltaic solar system by using two different MPPT algorithms, namely, perturb and observe (P&O) and incremental conductance (IC).

6.3 Conclusions

The proposed electro thermal model in Chapter 3, defines each heat path of the individual chip components for a multichip device. It was used to represent the actual behaviour of the power module in MATLAB/ Simulink. The proposed method is well-suited for monitoring the internal behaviour of the thermal effects within power electronic modules under their working conditions. The impact of the heat coupling effects among chips was found as high as 10 C° which was difficult to be accurately defined with most of the models in literature. Experimental real time verification of electro thermal model was achieved. The system determines IGBTs temperatures and heat distributions based on current and voltage measurements and embedded models. Based on this implementation, series of case studies applied for thermal performance comparison among SiC MOSFET and Si based IGBT devices within DC/DC boost converter. SiC device was found more thermally stable particularly at frequencies higher than 100 kHz and has approximately 20°C less operating temperature

characteristic compared to the IGBT devices on most of the tested conditions. However, current increase caused temperature inclination at lower frequencies. FSPT IGBTs performed the best at frequencies between 10-50 kHz thanks to their lower conduction loss characteristics. A model based solution to minimise the thermal effects and the induced stress of PECs in wind systems was implemented. IGBT junction's total temperature fluctuation were notably reduced; for FSIG by 12 °C, DFIG by 5 °C. Such temperature reduction leads to a total stress decrease by about 27 MPa. Experimental studies were conducted for a DC/AC inverter power module. Two case studies were performed in order to verify model based analysis. First, the inverter was fed by a constant power source under variable frequency operation. Then, an actual wind turbine system was used to apply variable speed/input operation to the coupled inverter. The thermal behaviour of inverter module during both cases was monitored by thermal imaging and dSPACE implementation. Good accuracy was obtained between model and experimental results for both cases. The estimated temperature data for variable wind operation was used to calculate number of cycles to failure and total life consumption of one of the chip wire bond. TLC as 1.88×10^{-5}, and it was observed that the higher speed caused more life consumption for the inverter.

Further analysis was studied for verification of the thermal stress deduction with the proposed switching frequency control method. Solder lifetime modelling was derived for the calculating the number of cycles to failure of the solder chips. The TLC was 4.25×10^{-5} for the fixed DC link operation. With the dynamic DC link operation, the TLC slightly decreased to 4.06×10^{-5}. With the proposed switching frequency control method significant TLC improvement was achieved especially by eliminating high temperature fluctuations. The TLC for this method was calculated as 3.26×10^{-5} which is approximately 1×10^{-5} less compared to the other both methods. Effects of IC and P&O maximum power point tracking algorithms on the electro thermal performance and lifetime of the IGBT used as switching element of PEC was presented. Compared to the P&O method, thermal cycling on the IGBT component was found as approximately 4°C higher when the IC method is operated and the steady state temperature was 52.7 °C while this was 42.6 °C with P&O. IC method was found to cause 1.4 more life consumption.

6.4 Future Work

The implemented electro thermal models and experimental work were verified by series of case studies. However, there are still many future work perspectives which would increase the overall accuracy and understanding the failure mechanisms of PECs. For instance, SiC technology could be further investigated based on its thermally beneficial material properties. Not only for IGBTs but also SiC Schottky diodes would offer better performance because of its lower forward drops and reverse recovery characteristics. More investigation towards SiC technology would lead manufacturing of multi-chip power devices which are very rarely available in market.

In terms of reliability enhancement, active cooling elements which monitor the device temperature and provides adjustments based on the certain temperature limits could be embedded within the PECs. By this way, online temperature control could be established. Although the electro thermal monitoring methods derived in this research are based on the online implementation of dSPACE system, the reliability models were derived with obtained temperature profiles using Simulink. The reliability models could be embedded within the online application of electro thermal model which would generate not only temperature but also online reliability modelling. The reliability models could be improved by considering more parameters which are relevant to failure mechanisms. For instance, the switching frequency could be considered while calculating the number of cycles to failure of a power electronic device.

In this research, the proposed switching frequency control technique for wind energy applications were derived by using SPWM method. This analysis could be expanded by implementing different modulation techniques i.e. SVM which would produce more thermal stress deductions; hence increase total life consumption. Electro thermal modelling of the DC-link capacitors can also be further implemented for lifetime consumption estimations of the power electronic converters.

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Appendix

Chapter 3

Heat Equation

Thermal and Electrical circuit parameters can be equated to each other in the theory of application. This can be proved by studying one dimensional heat diffusion equation for thermal and transmission line equation for electrical circuits. Applying the boundary conditions for both phenomena, direct conversion is mathematically established for the x-component of the heat equation as follows;

$$\frac{\partial^2 T}{\partial x^2} = \frac{p.c}{k}\frac{\partial \mathrm{T}}{\partial t} \tag{A.1}$$

When heat power, P_0 is applied to a solid object, equally distributed to area A, in the x-direction as shown in Fig. A.1, it is equivalent to A.5;

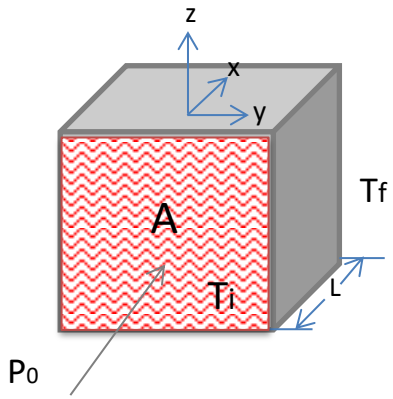


Figure A.1: Heat applied to solid object

$$P_0 = q.A \tag{A.2}$$

From (A.1); (A.5) can be written as:

$$P_0 = -k.A\,\frac{\partial \mathrm{T}}{\partial x} = -k.A\frac{\mathrm{Ts}-\mathrm{Tf}}{L} \tag{A.3}$$

Where L is the length of the total heated path, T_i is the initial (x=0) and T_f is final (x=L) temperature, through area, A. From (A.6), term $\frac{\mathrm{Tf}-\mathrm{Ts}}{Po}$ is defined as the Thermal Resistance, $R_{th}\ [K/W]$:

$$R_{th} = \frac{L}{k\,A} \tag{A.4}$$

The heat power P_0 can be interpreted as electrical current, since the Electrical Transmission Line Equation states:

$$\frac{\partial}{\partial x}\left(\frac{\partial \mathrm{V}}{\partial x}\right) = C_{el}L_{el}\,\frac{\partial}{\partial t}\left(\frac{\partial \mathrm{V}}{\partial t}\right) + (C_{el}R_{el} + G_{el}L_{el})\frac{\partial \mathrm{V}}{\partial t} + G_{el}R_{el}V \tag{A.5}$$

For an ideal transmission line with no inductance, L_{el}=0, and with an ideal isolation between two single lines, where the volume element cannot be cooled itself, G_{el}=0. Hence;

$$\frac{\partial^2 V}{\partial x^2} = R_{el}C_{el}\ \frac{\partial \mathrm{V}}{\partial t} \tag{A.6}$$

The electrical current $i(t)$ [A] as a function of voltages [V] is defined as:

$$i(t) = C_{el}.\frac{\partial \mathrm{V}}{\partial t} \tag{A.7}$$

By interpreting the electrical current as heat power and voltage as temperature in thermal domain (A.10) becomes;

$$p(t) = C_{th}.\frac{\partial \mathrm{T}}{\partial t} \tag{A.8}$$

Thermal Capacitance is defined as C_{th} $[J/K\ ]$, and from (A.1) & (A.9) it is represented as:

$$C_{th} = c.\rho.A.L \tag{A.9}$$

Hence (A.9) in thermal analysis, can be written as:

$$\frac{\partial^2 T}{\partial x^2} = R_{th}C_{th}\ \frac{\partial \mathrm{T}}{\partial t} \tag{A.10}$$

Table 1 shows the conversion between the parameters of the electrical and thermal systems.

Type	**Energy**	**Potential**	**Resistance**	**Capacitance**
Electrical	I, Current [A]	V, Voltage [V]	Rel, Electrical Resistance [Ω]	Cel, Electrical Capacitance [F]
Thermal	P, Dissipated Power [W]	T, Temperature [K]	Rth, Thermal Resistance [K/W]	Cth, Thermal Capacitance [J/K]

Table A.1: Electrical and Thermal System Parameters

The algorithm derived in Chapter 3 uses the analytical property of pure square roots, continued fraction equation [259] and its similarity between the nth order Cauer Form. Equations (A.14 to A.16) show the equivalence of Cauer Network when the number of layers attached together are increased.

$$Z_{th}(s) = \frac{1}{sC_1 + \frac{1}{R_1}} = \frac{1}{e + \frac{1}{f}} = \frac{f}{ef+1} \tag{A.11}$$

$$Z_{th}(s) = \frac{1}{sC_1 + \frac{1}{R_1 + \frac{1}{sC_2}}} = \frac{1}{d + \frac{1}{e + \frac{1}{f}}} = \frac{ef+1}{(de+1)f+d} \tag{A.12}$$

$$Z_{th}(s) = \frac{1}{sC_1 + \frac{1}{R_1 + \frac{1}{sC_2 + \frac{1}{R_2}}}} = \frac{1}{c + \frac{1}{d + \frac{1}{e + \frac{1}{f}}}} = \frac{(de+1)f+d}{(cde+c+e)f+cd+1} \tag{A.13}$$

$$\vdots$$

$$\vdots$$

The algorithm inputs the thermal capacitance and resistances of each layer from bottom to top and arranges the equivalence of nth layer form of Cauer. Then by coding, residue function of MATLAB finds the residues and poles of a partial fraction expansion of the ratio of two polynomials B(s)/A(s), that has a similar characteristics to Foster form as:

$$\frac{B(s)}{A(s)} = \frac{R(1)}{s - P(1)} + \frac{R(2)}{s - P(2)} + \cdots + \frac{R(n)}{s - P(n)} \tag{A.14}$$

where $R(n) = {}^{1}\!/_{C_{th}}$ and $P(n) = -{}^{1}\!/_{\tau}$ (A.15) &(A.16)

Analytical derivation of converted parameters for validation (for two RC elements) test can be derived as:

$$R_1' R_2' C_1' + R_1' R_2' C_2' = R_1 R_2 C_2 \tag{A.17}$$

$$R_1' C_1' + R_2' C_2' = R_1 C_1 + R_2 C_1 + R_2 C_2 \tag{A.18}$$

$$R_1' R_2' C_1' C_2' = R_1 R_2 C_1 C_2 \tag{A.19}$$

$$R_1' + R_2' = R_1 + R_2 \tag{A.20}$$

Solving A.20 to A.23, the validation of converted thermal parameters from Cauer to Foster can analytically be derived as:

$$R_1 = \frac{(R_2'\tau_1 + R_1'\tau_2)(C_1' + C_2')}{\tau_1 C_1' + \tau_2 C_2'} \quad \text{(A.21)}$$

$$C_1 = \frac{C_1' C_2'}{C_1' + C_2'} \quad \text{(A.22)}$$

$$R_2 = \frac{(\tau_1 - \tau_2)^2}{\tau_1 C_1' + \tau_2 C_2'} \quad \text{(A.23)}$$

$$C_2 = \frac{(\tau_1 C_1' + \tau_2 C_2')^2}{(C_1' + C_2')(\tau_1 - \tau_2)^2} \quad \text{(A.24)}$$

Where $\tau_1 = C_1' R_1'$ and $\tau_2 = C_2' R_2'$ (A.25 & 26)

To obtain the discrete equivalent of transfer function thermal impedance via numerical integration, system differential equation is written, then applied forward rectangular numerical integration technique as:

$$\dot{x}(k) \approx \frac{x(k+1) - x(k)}{T} \quad \text{(A.27)}$$

By transferring the above equation into frequency domain each discrete time left shift by n corresponds to a z^n multiplying factor in z-domain (see Fig A.2). Then, each d^n/dt^n in continuous time domain corresponds to a s^n multiplying factor in Laplace domain [260]. Thus it can be obtained as;

$$s \leftarrow \frac{z-1}{T} \quad \text{(Forward Rectangular Rule)} \quad \text{(A.28)}$$

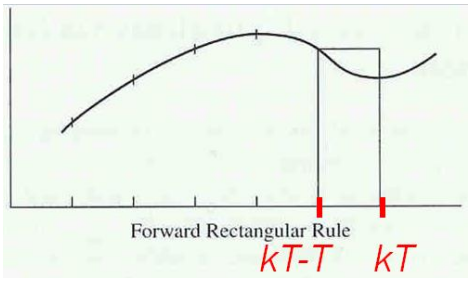


Figure A.2: Forward Rectangular Rule [260]

First Order Laplace form of the simple exponential term thermal model is:

$$Z_{th}(s) = R_{th} \,//\, 1/sC_{th} = \frac{R_{th}}{sR_{th}C_{th} + 1} = \frac{1/C_{th}}{s + 1/\tau} \quad \text{(A.29)}$$

The Forward Rectangular Euler's rule was applied to the thermal coefficients that were extracted in s-domain. The transfer function *H(s),* equivalent to (A.32), can be expressed in discrete domain as:

$$H(s) = \frac{b}{s+a} \rightarrow \quad H(z) = \frac{b}{\frac{z-1}{Ts}+a} \tag{A.33}$$

where $a = {}^{1}\!/_{C_{th}}$ and $b = {}^{1}\!/_{\tau}$ (A.34 & A.35)

The derivation of this analysis can be derived as [261]:

Transfer Function **Differential Equation**

$$\frac{U(s)}{E(s)} = H(s) = \frac{b}{s+a} \rightarrow \qquad \dot{u} = au = ae \tag{A.36}$$

In time continuous domain:

$$u(t) = \int_0^t (-au(\tau)+be(\tau))d\tau \tag{A.37}$$

In discrete time domain:

$$u(kT) = \int_0^{kT-T} (-au+be)d\tau + \int_{kT-T}^{kT} (-au+be)d\tau \tag{A.38}$$

$$u(kT) = u(kT-T) + \{areaof\,(-au+be)over\,[kT-T, kT[\} \tag{A.39}$$

From the Forward Rectangular Rule (Euler's Rule) with the approximation (kT –T);

The difference equation becomes [261]:

$$u_1(kT) = u_1(kT-T) + T[-au_1(kT-T)+be(kT-T)] \tag{A.40}$$

$$= (1-aT)u_1(kT-T) + bTe(kT-T) \tag{A.41}$$

Transfer Function:

$$U_1(z) = (1-aT)z^{-1}U_1(z) + bTz^{-1}E(z) \Rightarrow$$

$$H_F(z) = \frac{U_1(z)}{E(z)} = \frac{bTz^{-1}}{1-(1-aT)z^{-1}} = \frac{bT}{z-1+aT} = \frac{b}{\frac{z-1}{T}+a} \tag{A.42}$$

By equating (A.32) where $a = 1/C$, $b = 1/\tau$ and $\tau = RC$

$$Z_{th}(z) = \frac{\frac{1}{C}}{\left(\frac{z-1}{T}\right)+\frac{1}{RC}} = \frac{\frac{1}{C}}{\frac{RC(z-1)+T}{TRC}} = \frac{TR}{RC(z-1)+T} \tag{A.43}$$

Applying a heat source, P, to thermal impedance (A.32), change in the temperature, ΔT, in s-domain yields the following expression:

$$\Delta T = \frac{1/C}{s+1/RC} P \tag{A.44}$$

In z-domain:

$$\Delta T = \frac{TR}{RC(z-1)+T} P \tag{A.45}$$

$$\frac{\Delta TRC(z-1)}{T} = RP - \Delta T \tag{A.46}$$

$$\Delta T = \frac{P}{C\left(\frac{Z-1}{T}\right)} - \frac{\Delta T}{RC\left(\frac{Z-1}{T}\right)} \tag{A.47}$$

Average vs Instantaneous Power Loss

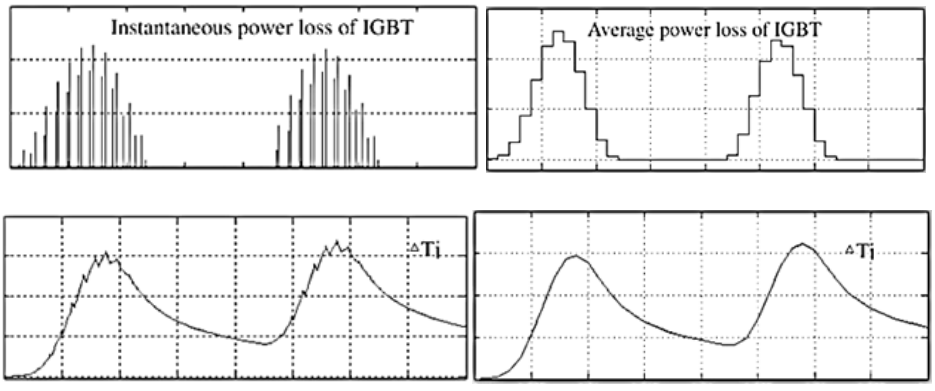
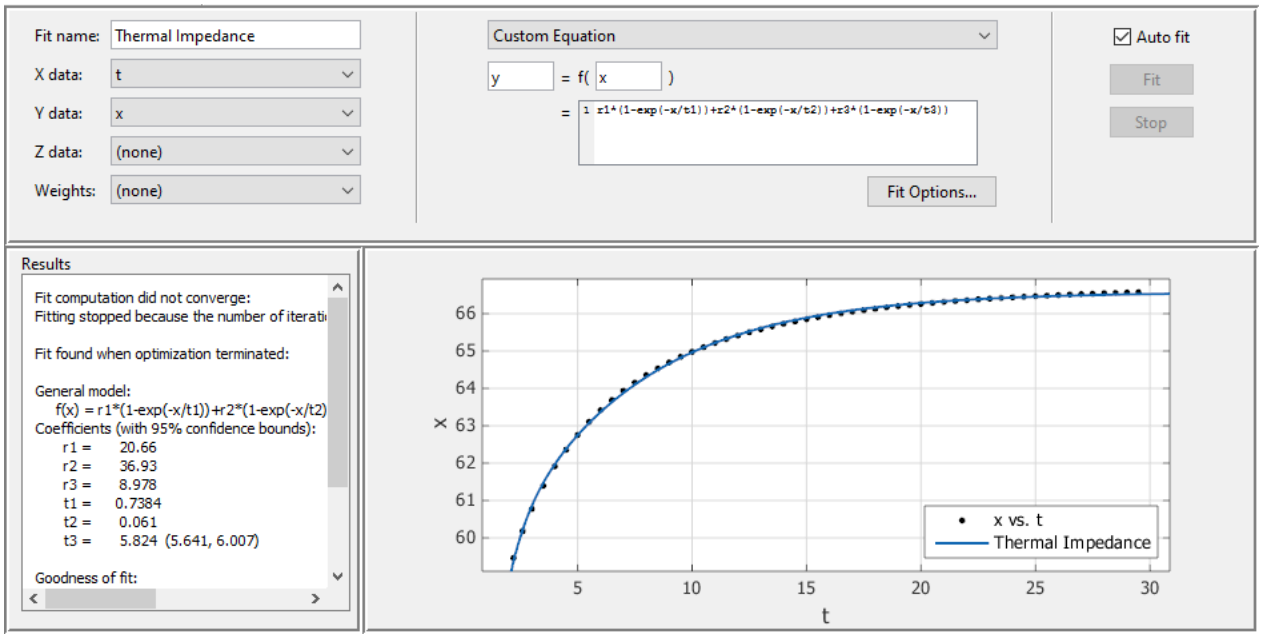


Figure A.3: Instantaneous and Average Power loss data with respect to temperature

Curve Fitting in Matlab



Boost Converter Design

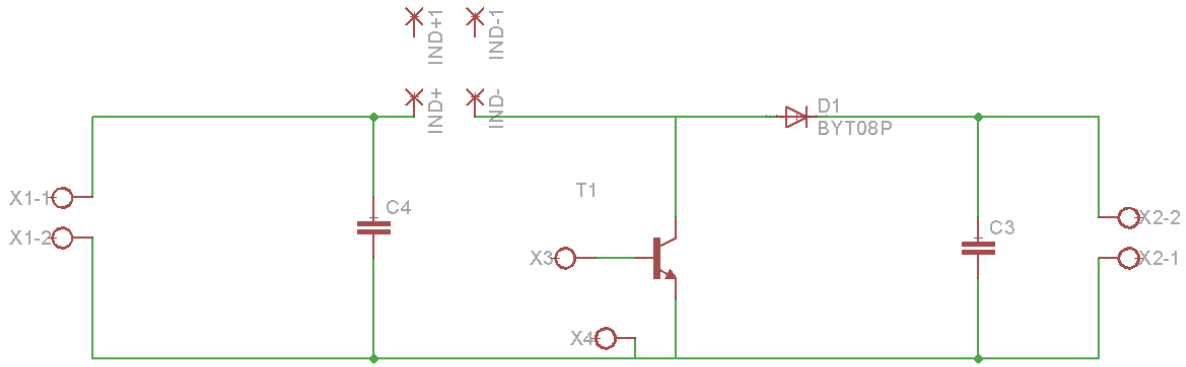


Figure A4: Boost Converter Schematic

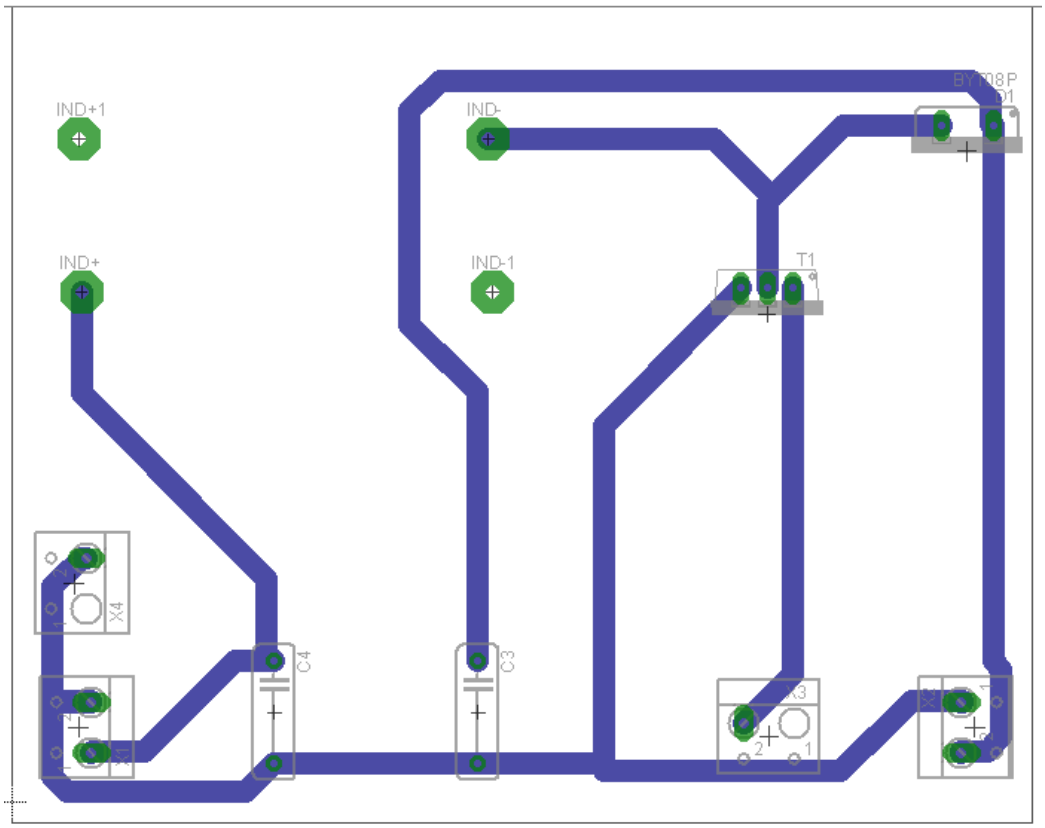


Figure A5: Boost Converter PCB Layout

Driver Circuit Design

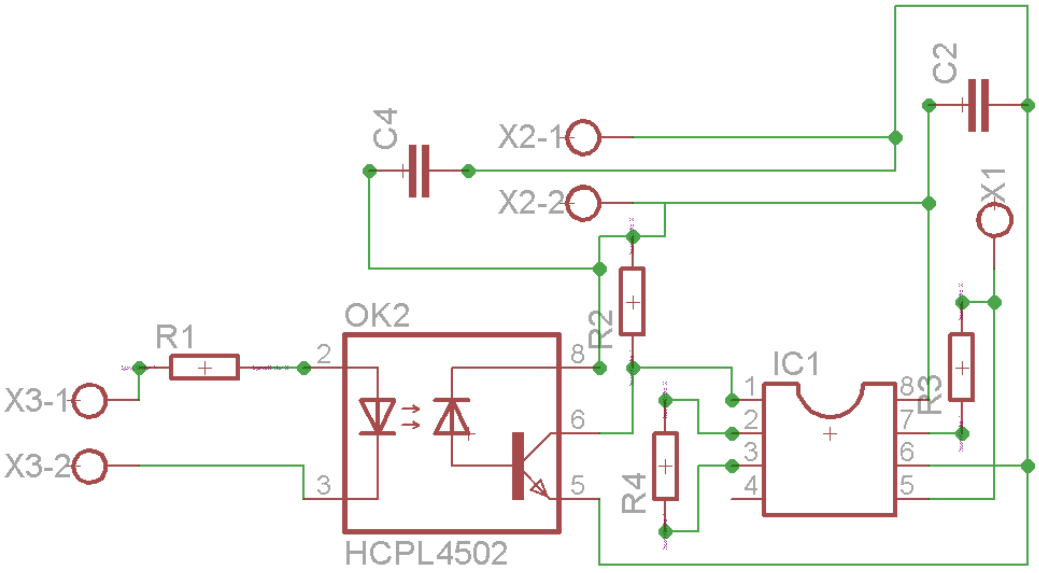


Figure A6: Driver Schematic

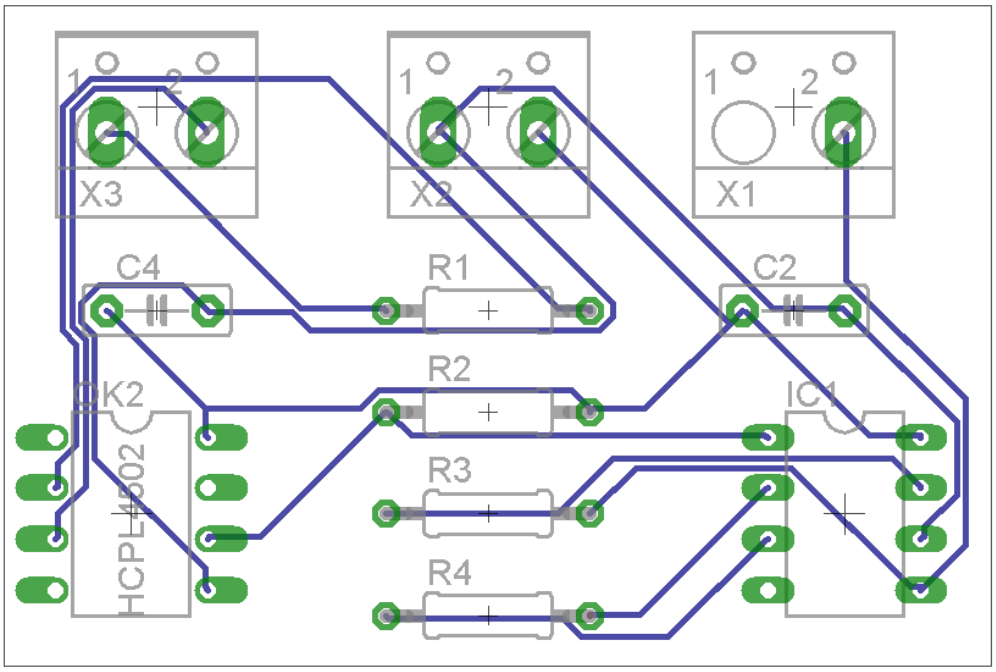


Figure A7: Driver PCB Layout

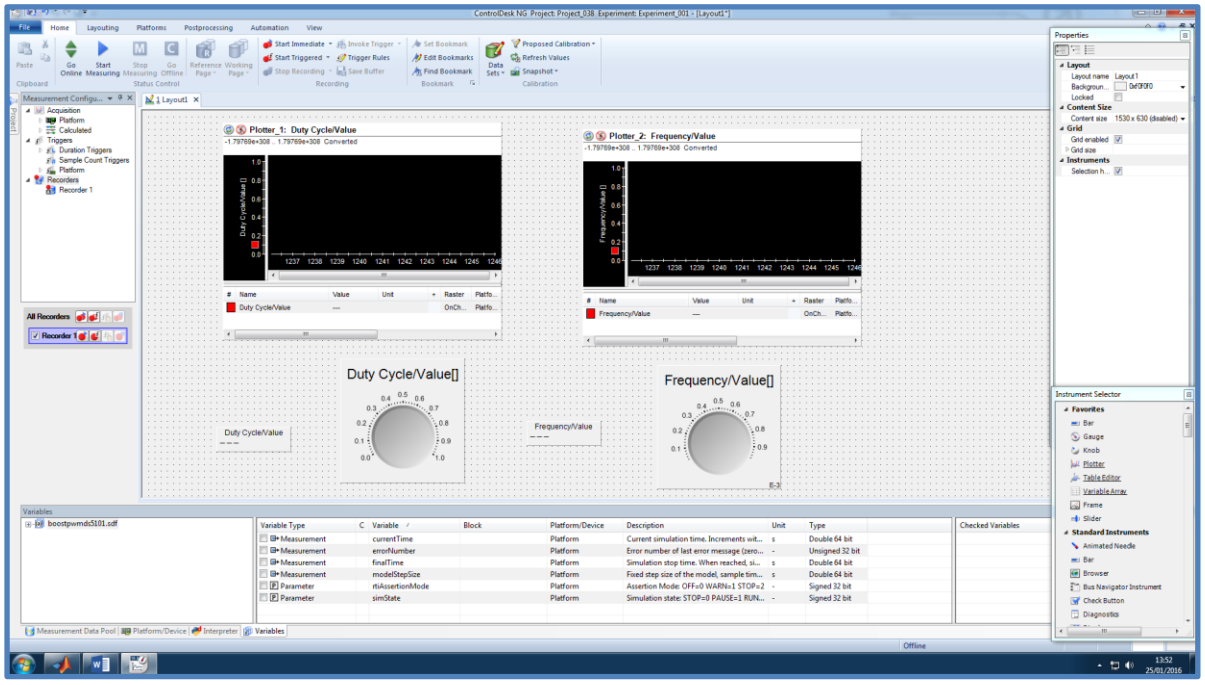


Figure A8: dSPACE Control desk

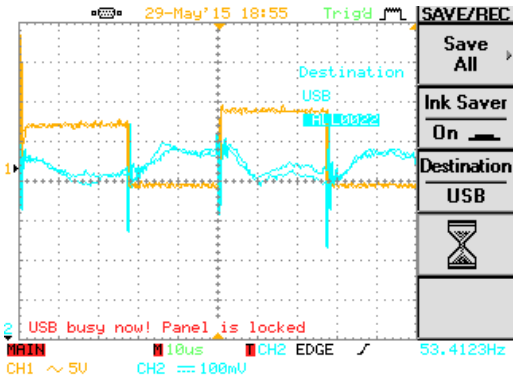


Figure A9: Opt coupler signal vs. collector current

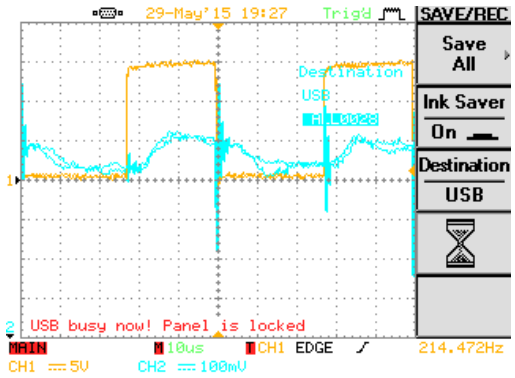


Figure A10: Driver Gate signal vs. collector current

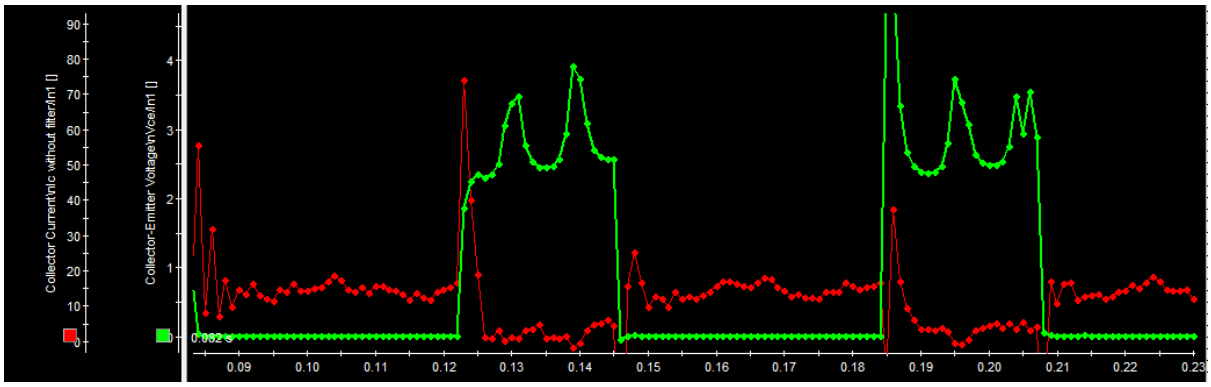


Figure A11: Collector current and voltage in dSPACE Control Desk

Chapter 4

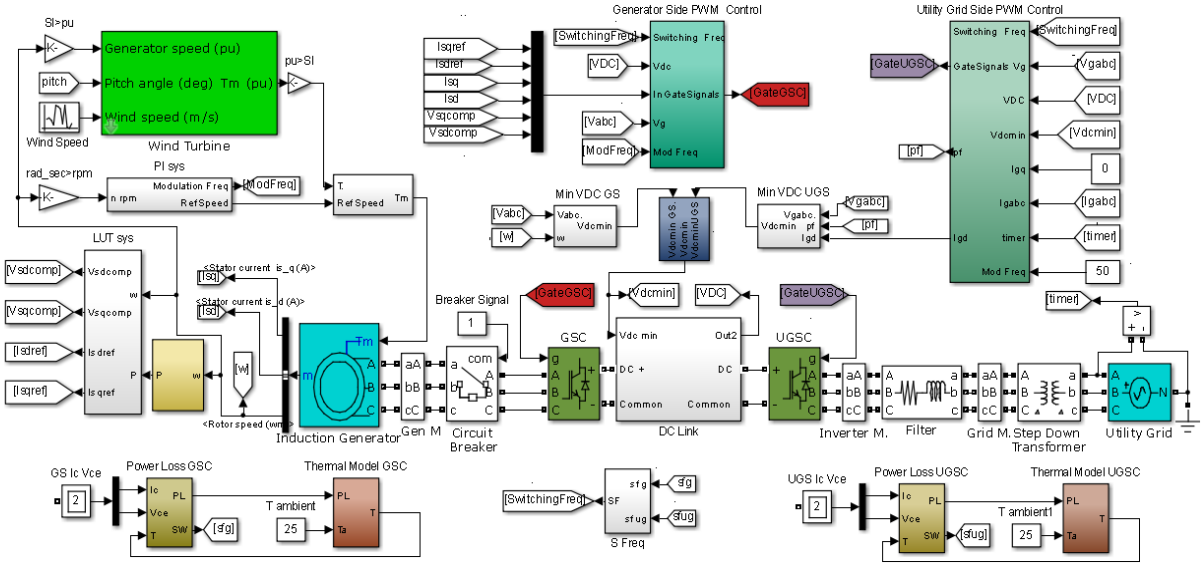


Figure A.12 Simulink Model view for FS based with systems

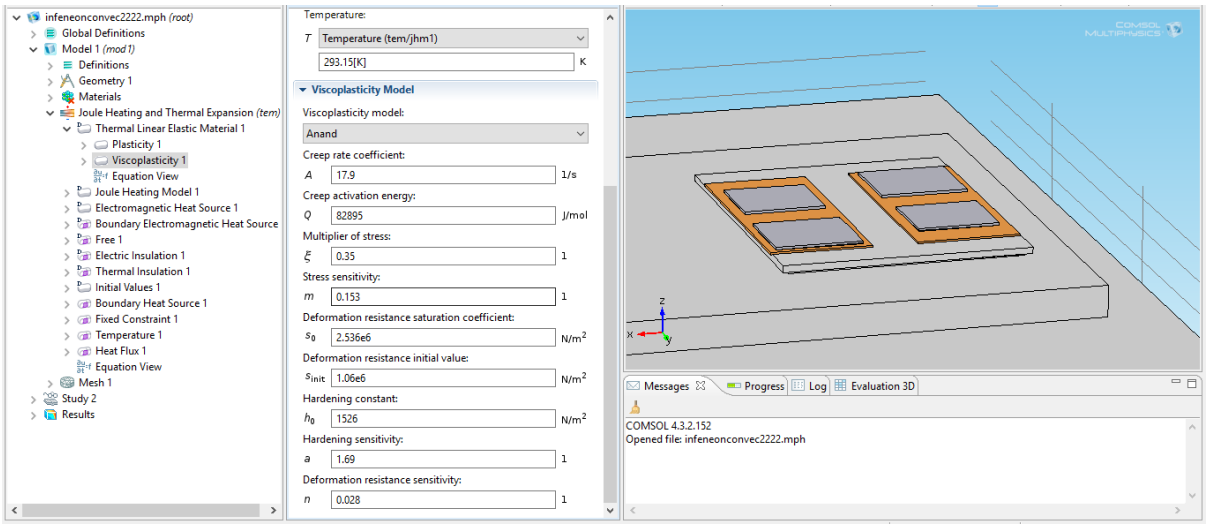


Figure A.13 Anand viscoplasticity model in COMSOL

Chapter 5

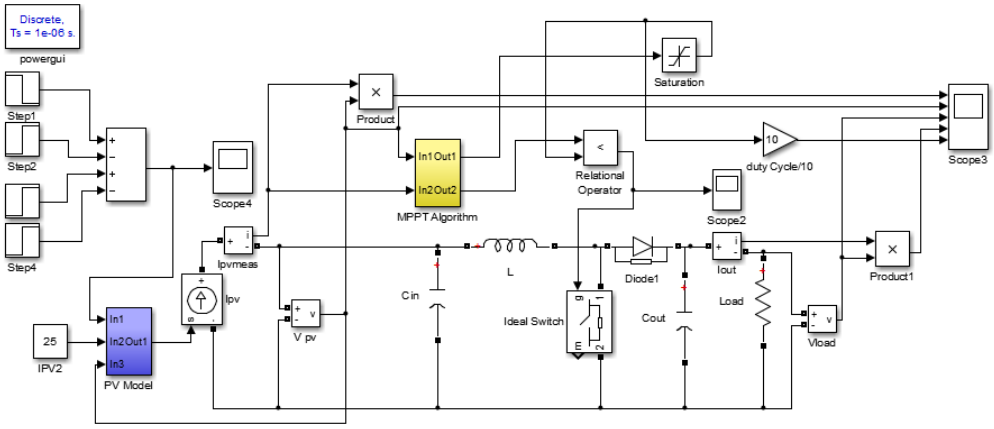
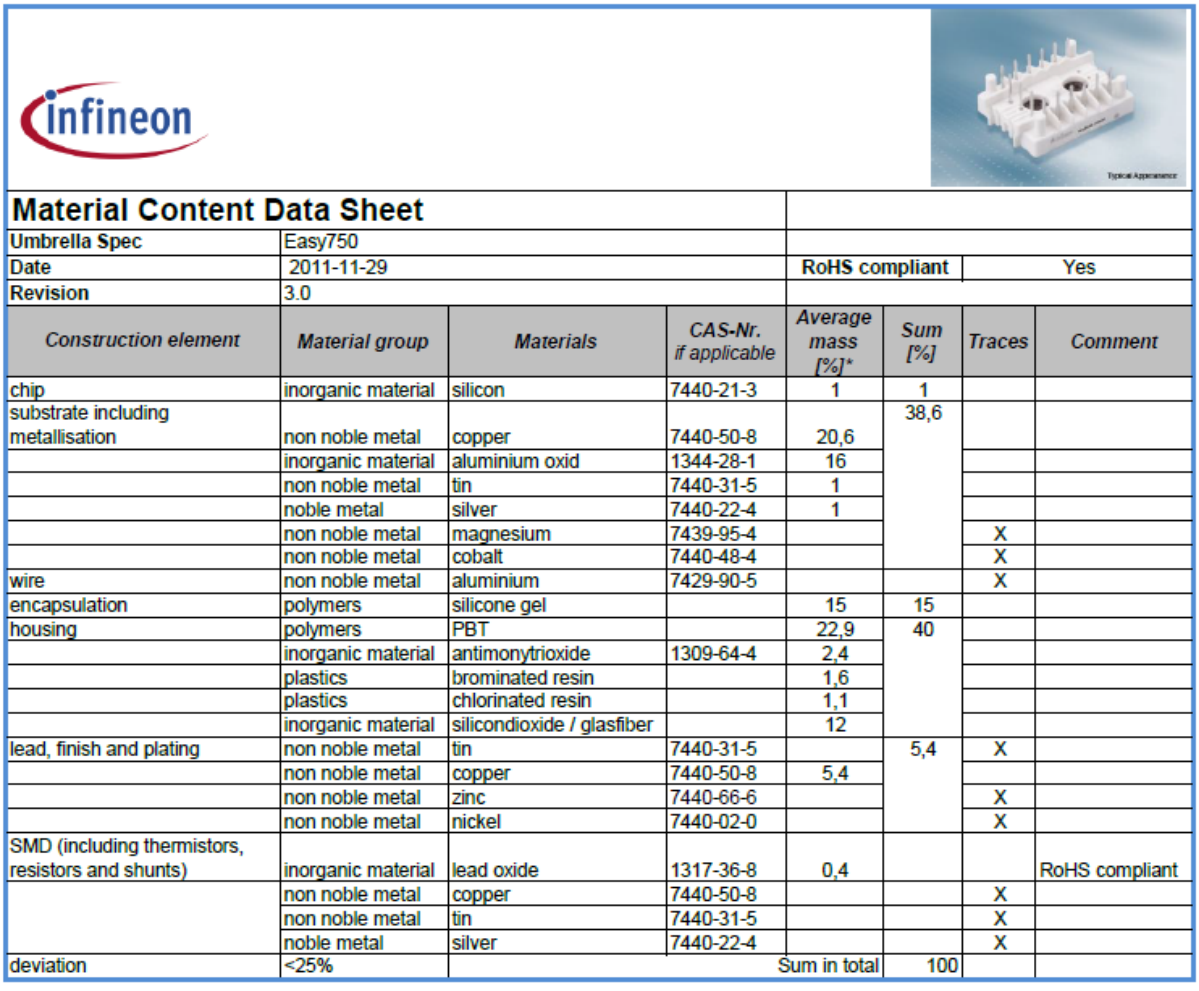


Figure A.14: Simulink model of PV system simulation



Material Content Data Sheet

Umbrella Spec	Easy750						
Date	2011-11-29			**RoHS compliant**		Yes	
Revision	3.0						
Construction element	*Material group*	*Materials*	*CAS-Nr. if applicable*	*Average mass [%]**	*Sum [%]*	*Traces*	*Comment*
chip	inorganic material	silicon	7440-21-3	1	1		
substrate including metallisation	non noble metal	copper	7440-50-8	20,6	38,6		
	inorganic material	aluminium oxid	1344-28-1	16			
	non noble metal	tin	7440-31-5	1			
	noble metal	silver	7440-22-4	1			
	non noble metal	magnesium	7439-95-4			X	
	non noble metal	cobalt	7440-48-4			X	
wire	non noble metal	aluminium	7429-90-5			X	
encapsulation	polymers	silicone gel		15	15		
housing	polymers	PBT		22,9	40		
	inorganic material	antimonytrioxide	1309-64-4	2,4			
	plastics	brominated resin		1,6			
	plastics	chlorinated resin		1,1			
	inorganic material	silicondioxide / glasfiber		12			
lead, finish and plating	non noble metal	tin	7440-31-5		5,4	X	
	non noble metal	copper	7440-50-8	5,4			
	non noble metal	zinc	7440-66-6			X	
	non noble metal	nickel	7440-02-0			X	
SMD (including thermistors, resistors and shunts)	inorganic material	lead oxide	1317-36-8	0,4			RoHS compliant
	non noble metal	copper	7440-50-8			X	
	non noble metal	tin	7440-31-5			X	
	noble metal	silver	7440-22-4			X	
deviation	<25%			Sum in total	100		

Figure A.15: Inverter Materials